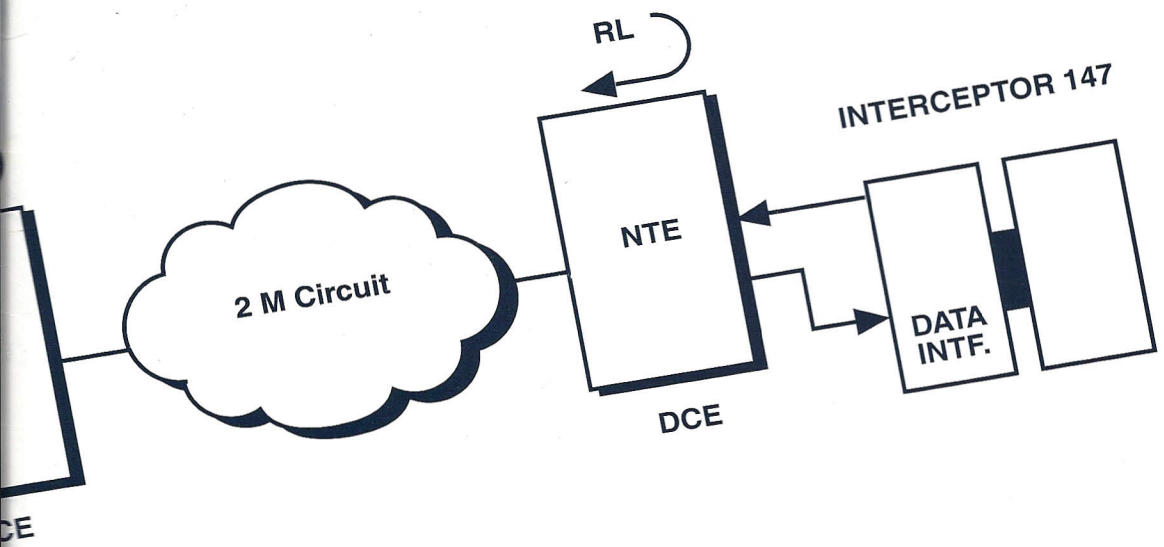
INTERCEPTOR® 147

Testing Data Communications Circuits

Application Note



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Testing Data Communications Circuits with the TTC INTERCEPTOR® 147

Overview

Data communications, such as the transmission of computer information, play an increasingly important role in today's networks. The growth in data traffic presents new challenges and applications for testing. The test requirements for data communications are handled differently from those of voice.

This ***Application Note*** briefly describes data communications circuits, and presents an overview of testing these circuits with the TTC INTERCEPTOR 147 Communications Analyzer. The INTERCEPTOR 147 is a hand-held analyzer that is designed for solving data communications problems in the field.

1. Data Communications Testing

Transmission systems, which were originally designed to carry voice signals, now transport a considerable amount of data. In general, error performance in data systems is more critical than in voice systems. For example, data circuits should provide an error rate lower than 10^6, or 1 errored bit in every 1,000,000 bits; voice signals can tolerate error rates as high as 10^3, or 1 error in every 1,000 bits transmitted. Therefore, data circuits' requirement for clean lines is 1,000 times more stringent than those of voice. This section describes data communications circuits, data interfaces, data equipment and terminology, and testing at the data interface.

A. Data Communications Circuits

In order for computer information to flow between two points, a proper electrical circuit must be established. The basic component that defines this circuit is known as the *data interface*. The data interface consists of the input and output circuitry and, ultimately, the physical medium that allows data communications to occur.

The INTERCEPTOR 147 enables you to test at five common data interfaces. ***Table 1*** lists these interfaces, and describes where each is used.

Interface:	Description:
V.24/RS-232C	Used for bit rates up to 20 kbit/s. It is known as V.24 in Europe or as RS-232C in North America.
V.35	Originally used for bit rates up to 48 kbit/s, but is now used for 2048 kbit/s and higher.
G.703 64 kbit/s Codirectional	Used for 64 kbit/s fractions of the 2048 kbit/s signal.
X.21	Used for synchronous mode in data networks for bit rates from 600 bit/s to 2048 kbit/s.
V.11/RS-449	Used for bit rates up to 2048 kbit/s. It is known as V.11 in Europe or as RS-449 in North America.

Table 1 Data interfaces and their uses.

Most important to this process are the standards that define this physical interface – without these standards, no common rules would exist. Each data interface has an electrical, functional, and mechanical specification. These specifications are defined by international groups, such as the International Telegraph and Telephone Consultative Committee (CCITT, now called ITU-T) and Electronic Industries Association (EIA), and by regulatory bodies in many countries. The function of the specification is to define the requirements for these interfaces, and to ensure compatibility among equipment vendors. Without this compatibility, communications networks could not function properly.

Electrical Specifications

The electrical specifications describe the signals across the interface. These include voltage and current levels, loopback definitions, and timing (clock) considerations.

Functional Specifications

The functional specifications for an interface determine the functional role of each signal. For our purposes, this is contained in the pin assignments for the interfaces. Refer to Appendix A for a description of the pin assignments for the interfaces that the INTERCEPTOR 147 supports.

Mechanical Specifications

The mechanical specifications for an interface describe its basic characteristics. These include the shape of the connector, pin arrangements, assignment of signals to connector pins, connector gender, and cable characteristics.

B. Equipment and Terminology

Essential to understanding data communications is an understanding of the key terminology. Terms, such as DTE, DCE, signaling leads, and timing are used frequently, but their meanings are not always intuitive. This section defines DTE and DCE, signaling leads, and synchronous and asynchronous timing modes.

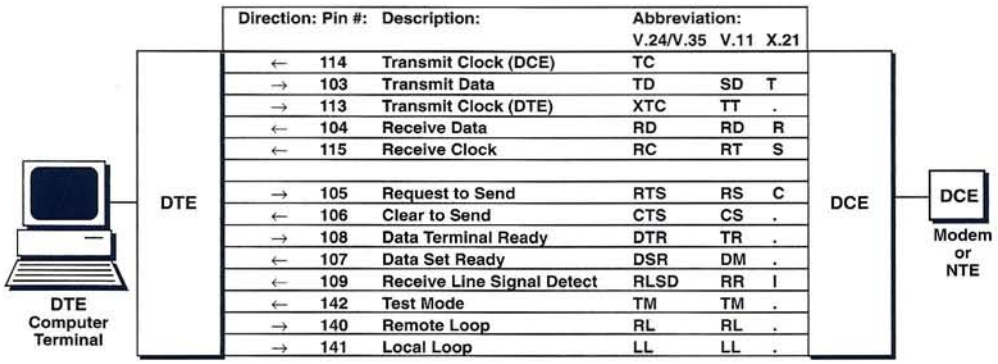
DTE and DCE

The data circuit is composed of essentially two types of equipment. The equipment on either end of a circuit that *generates* or receives the information being moved is called the Data Terminal Equipment (DTE). DTE can be any device that is able to transmit or receive data. The equipment that *passes* the signal from place to place is the Data Circuit Terminating Equipment, also called Data Communications Equipment (DCE). The determination of whether a device is a DTE or DCE depends upon perspective, or where the equipment is located along the communications path. Typically, the DCE controls the clock function. A basic example of a DTE is a computer, and an example of a DCE is a modem. A computer is a source of the information that it transmits or receives; a modem simply moves the information to the next point.

The interface between a DTE and a DCE is called the transmission channel or line. This channel size depends on how much bandwidth is required by DTE. The transmission channel can be as short as a patch cord, or can span the globe as part of an international network.

Lead Description and Control

The transfer of information between DCEs and DTEs is controlled through signaling leads. The individual interface standards cover the assignment of signals to connector pins, or *leads*. Some of these leads are common to all data interfaces. ***Figure 1*** shows the data communications control leads.



Direction:	Pin #:	Description:	Abbreviation: V.24/V.35	V.11	X.21
←	114	Transmit Clock (DCE)	TC		
→	103	Transmit Data	TD	SD	T
→	113	Transmit Clock (DTE)	XTC	TT	.
←	104	Receive Data	RD	RD	R
←	115	Receive Clock	RC	RT	S
→	105	Request to Send	RTS	RS	C
←	106	Clear to Send	CTS	CS	.
→	108	Data Terminal Ready	DTR	TR	.
←	107	Data Set Ready	DSR	DM	.
←	109	Receive Line Signal Detect	RLSD	RR	I
←	142	Test Mode	TM	TM	.
→	140	Remote Loop	RL	RL	.
→	141	Local Loop	LL	LL	.

Figure 1
Data communications interface leads.

Table 2 is a brief description of the leads used on the V.24, V.35, V.11, and X.21 interfaces.

Lead:	Description:
Transmit Clock (DCE)	This lead is used by the DTE to control bit timing, and allows the DCE to originate clocking.
Transmit Data	The DTE transmits binary data on this lead.
Transmit Clock (DTE)	This lead is sent by the DTE to control bit timing. The DCE will use this in a special timing mode.
Receive Data	The DTE receives binary data on this lead.
Receive Clock	This lead is bit-synchronous with receive data.
Request to Send	This lead is sent by the DTE to request that the transmission process begins.
Clear to Send	Sent by the DCE to allow the DTE to transmit data, terminals may not transmit until a CTS signal is received from the DCE.
Data Terminal Ready	The DTE sends this to indicate that it is ready to receive data from the DCE.
Data Set Ready	This indicates that the data set (i.e., DCE) is ready to receive data.
Receive Line Signal Detector	This signal is sent by the DCE to indicate that the transmission line signal has been detected.
Test Mode	This is sent by the local DCE to indicate that a loopback is being performed.
Remote Loop	The DTE sends this to initiate a loopback of the far-end DCE.
Local Loop	The DTE sends this to initiate a loopback of the near-end DCE.

Table 2
Lead descriptions.

Synchronous and Asynchronous Timing Modes

The receiving equipment must know when to look for incoming data signals in order for a data transmission system to work properly. Coordination between the transmitting and receiving equipment is essential, so that data bits are not accidentally added or deleted during the transfer of information. The places where this coordination takes place are in the transmitter's and receiver's clocks, so this coordination is referred to as *timing*. The two common timing methods used for data communications are asynchronous and synchronous timing.

Asynchronous timing maintains synchronization on a character-by-character basis, using start and stop bits. Asynchronous characters can be 5, 6, 7, or 8 bits long. Each character begins with a start bit and ends with a stop bit that establishes receiver timing. Asynchronous timing is embedded in the data.

Synchronous timing transmits a block of characters as a continuous bit stream. A separate timing signal (sent by the transmitter, although the source of this timing can be a DTE or DCE) coordinates this transmission. Once the data is multiplexed into a 2 Mbit/s or G.703 signal, the timing mode is isochronous.

Isochronous transmission is a form of synchronous transmission, where no separate clock signal is passed between the transmitter and receiver. Instead, the clock is embedded in the data stream, and the receiver recovers timing from the data stream. ***Figure 2*** illustrates the difference among asynchronous, synchronous, and isochronous timing.

For more information on timing, refer to the *Solving Network Timing Problems Application Note* from TTC.

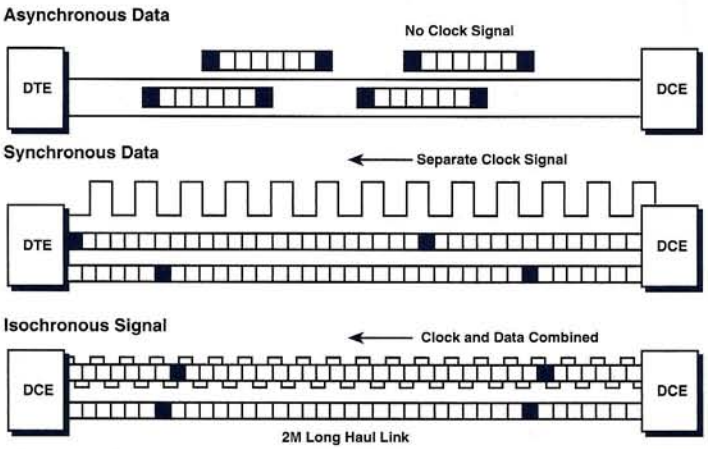


Figure 2
Asynchronous, synchronous, and isochronous timing.

C. Testing at the Data Interface

In order to maintain and verify the quality of data communications circuits, focused testing at the data interface is required. This section provides an overview of test considerations at the data interface.

Lead Exchange and Lead Delay

Before information can pass between a DTE and a DCE, the proper control leads must be exchanged. This exchange of pre-determined signals is called a *handshake*, since it occurs when a connection between the devices is first established, and is used to determine that the DTE and DCE are ready to exchange data.

Signal-lead timing relationships at the DCE-to-DTE interface are important, in particular the delay between two lead state changes. One example is the Request to Send/Clear to Send (RTS/CTS) delay measurement.

The handshake exchange is initialized by the DTE and DCE raising their DTR and DSR leads, to notify each other that they are in place and ready to pass data. Information begins to flow when the DTE and DCE exchange their respective RTS and CTS leads.

RTS / CTS delay measurement is the time between the DTE setting the RTS on, and the DCE setting CTS on as a response. Data is only transferred when CTS is on, so too long a delay reduces data throughput. Too short a delay can result in data being lost, because the DCE or DTE may not be ready to proceed. Typically, lead delay times for data circuits range from 10 to 100 milliseconds.

Lead Status LEDs on the INTERCEPTOR 147 allow instant monitoring of the CTS, RTS, DSR, DTR, RD, RC, (for X.21, also C and I), LL, and RL leads.

Generator Clock and Receive Clock Configuration

The type of clock used by the network components has a large impact on how the network operates. Some types of equipment, for example, drift out of specification and create clock problems.

The INTERCEPTOR 147's Generator Clock (Gen Clk) function selects the clock source used for data interface testing; and the Receive Clock (Rcv Clk) function selects the clock that supplies timing for data received on the data interface.

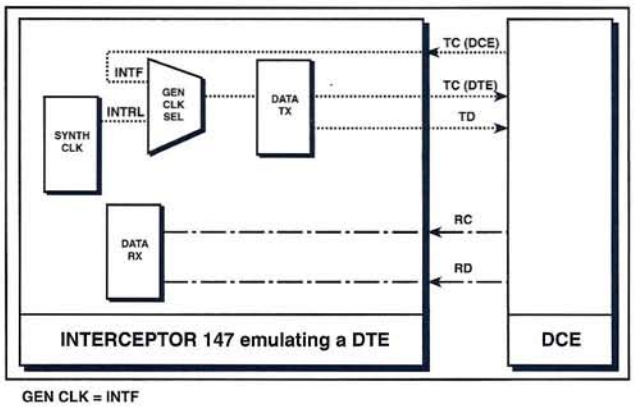
The Generator Clock Select (Gen Clk Sel) function has two functions that specify the source, either Internal (INTRNL) or Interface (INTF). The INTRNL function sets the transmit timing source as the INTERCEPTOR 147's internal clock; the INTF function sets the transmit timing source as the received signal or clock.

The Receive Clock Select (Rcv Clk Sel) function has two timing functions, Transmit Timing (TT) and Send Timing (ST). When emulating DCE, the TT signal from the DTE (see ***Figure 3***) is normally used; if TT is not active, then ST is used. In ST mode, the INTERCEPTOR 147 generates its own internal clock, uses this clock to time received data, and transmits it to the DTE on the Transmit Signal Element Timing (TC) lead; the INTERCEPTOR 147 receives the clock from the DTE on the Transmit Timing lead, and uses it to time its received data.

Polarity refers to the sense of the clock pulses, which is either positive or negative. The INTERCEPTOR 147's Send Clock Polarity (Send Clk Pol) function selects the polarity of the clock that times transmit data; the Receive Clock Polarity (Rcv Clk Pol) function selects the polarity of the clock that samples received data.

The Send Clk Pol's Normal (NORM) selection generates data on the falling edge of the clock; the Inverted (INV) selection generates data on the rising edge of the clock. The Rcv Clk Pol's Normal (NORM) selection samples data on the falling edge of the clock; the Inverted (INV) selection samples data on the rising edge of the clock.

Figure 3 shows the Generator Clock and Receive Clock configurations on the INTERCEPTOR 147.



Loopback and End-to-End Test Configurations

One of the basic techniques for isolating faults in data communications is the loopback test. In a loopback, the output at the far end of a system is connected to the input of the return path. The output of the return path is examined and compared to the input of the outgoing path. A benefit of the loopback test is it can be performed by one technician at one location, as opposed to an end-to-end test which requires coordination between two technicians. End-to-end (sometimes called full-duplex) testing analyzes the data link in both transmit and receive directions. The end-to-end test provides the best Physical Layer error check of circuits and equipment. It is superior to loopback tests since it provides problem isolation to either the transmit or receive path, which improves sectionalization capabilities. In addition, end-to-end testing can locate problems that may be corrected by the transmission equipment (e.g., CRCs, frame, and code errors) in a loopback configuration.

You can use the INTERCEPTOR 147 to test data interfaces by replacing DCE or DTE such as a terminal or multiplexer, and conducting a complete Bit Error test. See ***Figure 4*** for a diagram of a typical test setup.

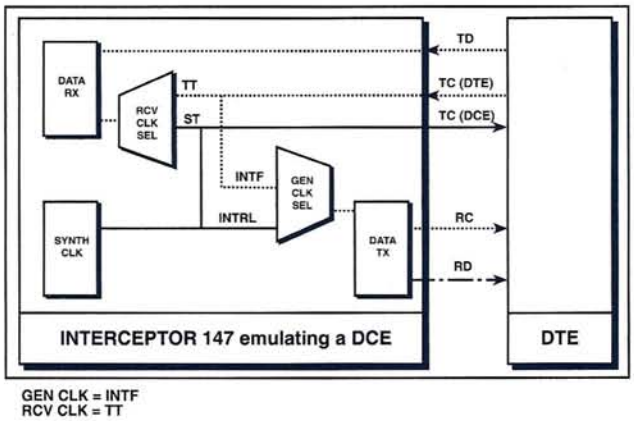


Figure 3
Gen Clk and Rcv Clk configurations.

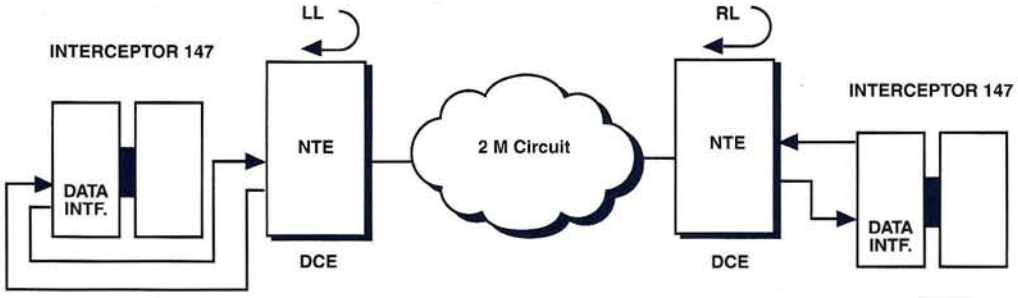


Figure 4
Testing data circuits.

Test Setup

1. **TEST MODE** category.
   Set Test Mode to **DATA**. Set **Intf** to the interface used on the interface under test.

2. **CONFIGURATION** category.
   In the Data Lead item, set RTS and DTR to **ON**. Set LL and RL to **OFF**. Alternately, local and remote loopbacks (LL and RL) may be initiated and used to sectionalize the circuit (V.24, V.35, and V.11 interfaces only).

3. **AUXILIARY** category.
   If you are using a printer, set all printer-related functions as desired. Make sure that **Time** and **Date** are set for the correct time and date.

4. Data Interface connector.
   Using the appropriate data interface connector, connect the INTERCEPTOR 147 to the circuit under test.

Test Results

1. Watch the **DATA INTERFACE** LEDs to verify that the proper DTE/DCE exchange takes place. Check the **STATUS & ALARMS** LEDs to verify proper detection of signal, pattern, and absence of alarms.

2. Insert a bit error to verify an end-to-end test or loopback configuration . Press **Restart**.

3. Check the **SUMMARY** Results category to see if any Bit Errors or Pattern Slips have occurred. The **Results OK** display indicates there are no errors.

4. In the **SIGNAL, CODE & FAS** Results category's Freq item, verify the receive frequency for the proper rate and check for evidence of drift. Drift is ΔPPM Results and Rcv Freq variation. If there are changes, then drift occurred.

5. Check the results in the **PERFORMANCE** Results (G.821) category to determine the overall quality of the circuit.

6. Loopback the circuit at a different point, and repeat the test.

Test Benefits

The benefit of this test is that the INTERCEPTOR 147 replaces a network element to thoroughly verify the end-to-end performance of the data circuits. This can be used to confirm the integrity of the Physical Layer throughout the network, and to differentiate Physical Layer problems from protocol problems.

2. Multiplexer Testing

A multiplexer (mux) is a device that allows several data channels to be combined into one physical circuit. The data streams that are combined in a multiplexer can be recovered and separated at the opposite end of a system. The INTERCEPTOR 147 can be used to test a mux in a variety of ways. This section describes mux wrapping, and mux and demultiplexer (demux) testing, including data to 2 Mbit/s and 2 Mbit/s to data.

A. Performing a Wrap-Around Test

A testing technique known as *Mux wrapping* involves simultaneously testing at both the data and line side of a 2 Mbit/s multiplexer.

Test Benefits

Mux wrapping performs several functions. It serves to verify the data stream-to-network multiplexing, to to assure timing recovery from the network by the mux, and assure timeslot and bandwidth mapping to the data interface. Additionally, mux wrapping can be used as a method of stress testing the multiplexer.

B. Mux and Demux Testing

When a multiplexer is faulty, it must be tested out-of-service. The two methods of verifying data transfer through the multiplexer are mux and demux testing. Mux testing can be an in-service test (except for the data port and 2 M timeslot which are used) that inserts a test pattern onto a data circuit, and verifies that the information is being properly channelized. Demux testing is an out-of-service test that transmits a 2 Mbit/s signal and then demultiplexes it on the data side, to verify that data is being received.

Data to 2 Mbit/s

A mux test inserts a test pattern onto a data circuit, and verifies that the information is framed correctly. This may be done in service with the 2 M receiver at a bridge or monitor point. ***Figure 5*** shows a data to 2 Mbit/s test.

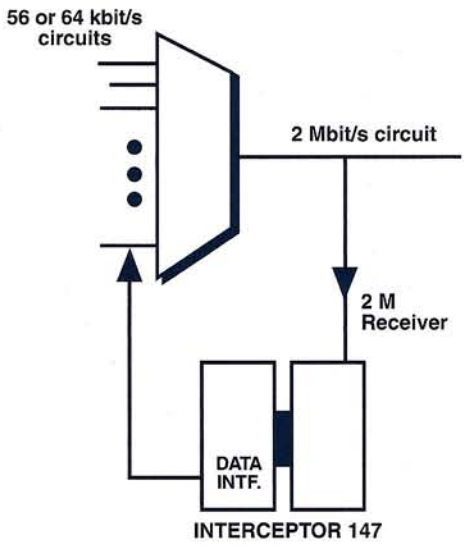


Figure 5
Data to 2 Mbit/s.

Test Setup

1. **TEST MODE** category.
   Set Test to **MUX**.
   Use the TX >RX item to specify whether you are performing a mux or demux test. Set the display to DATA > 2 M.
   Set **Intf** to the interface used on the data circuit.
   Set **2 M** to the bandwidth used on the 2 Mbit/s timeslot.
   Set **Gen Clk** to INTF, to use the interface as the clock source.

2. **CONFIGURATION** category.
   Set **Framing** to the format used on the 2.048 Mbit/s link under test (or set Framing to **AUTO**). Set the Data Leads and Pattern.

3. **TIMESLOTS** category.
   Select the timeslot onto which you expect the data to be multiplexed onto the 2 Mbit/s side.

4. **AUXILIARY** category.
   If you're using a printer, set all printer-related items as necessary. Make sure that **Time** and **Date** are set for the correct time and date.

5. **RECEIVER** control.
   Press the **RECEIVER** control to select **MON**, **TERM**, or **BRIDGE**, and **120Ω** or **75Ω**, as appropriate.

6. **RECEIVER** connector
   Using the **120Ω** or **75Ω RECEIVER** connector, connect the INTERCEPTOR 147 to the 2 Mbit/s transmit side of the multiplexer under test.

7. Data Interface connectors.
   Using the appropriate data interface connector, connect the INTERCEPTOR 147 to the multiplexer under test.

Test Results

1. Watch the **DATA INTERFACE** LEDs to verify that the proper DTE/DCE lead exchange occurs. Check the **STATUS & ALARMS** LEDs to verify proper detection of signal, framing, pattern, and absence of alarms. Pattern Sync indicates proper channel mapping.

2. In the **SUMMARY** Results category, check for the occurrence of any error conditions.

3. To check circuit continuity, transmit a bit error and verify that it is received (check the Bit Errs item in the **LOGIC & TIME** Results category). Press **Restart**.

4. In the **SIGNAL, CODE & FAS** Results category, check Freq and Freq Δppm to verify that the receive frequency is at the proper rate and to check for evidence of drift. Drift is ΔPPM Results and Rcv Freq variation. If there are changes, then drift occurs. Also check Level (dBnom) and Level (Vpeak) to verify proper levels.

5. In the **PERFORMANCE** Results category, the G.821 Performance results provide an excellent means of verifying the overall quality of the link under test.

2 M to Data

A demux test transmits a 2 Mbit/s signal and then demultiplexes it on the data side. This way, you can verify that data is being received. This is an out-of-service test because it is intrusive on the 2 M line. ***Figure 6*** shows a 2 Mbit/s to data test.

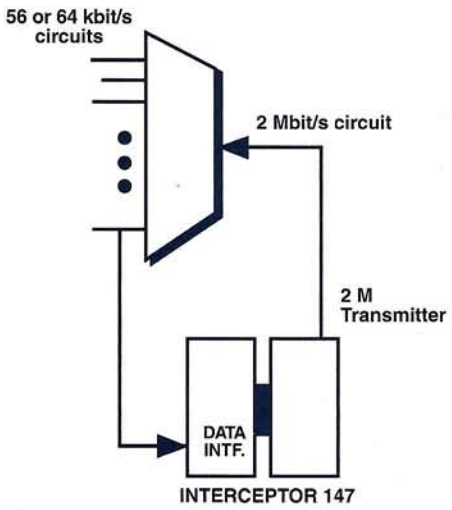


Figure 6
2Mbit/s to Data.

Test Setup

1. **TEST MODE** category.
   Set Test Mode to **MUX**.
   Use the TX > RX item to specify whether you are performing a mux or demux test. Set the display to 2 M > DATA.
   Set **Intf** to the interface used on the data circuit.
   Set **2** M to the bandwidth used on the 2 Mbit/s circuit.

2. **CONFIGURATION** category.
   Set Framing to that of the mux under test. Set Data Leads RTS and DTR to **ON**. Set LL and RL to **OFF**.
   Select a Test Pattern. Set Gen Clk to **Internal**.

3. **TIMESLOTS** category.
   Select the timeslots which are to be demultiplexed from the 2 Mbit/s circuit mapped to the data interface under test.

4. **AUXILIARY** category.
   If you are using a printer, set all printer-related setup items as desired. Make sure that **Time** and **Date** are set for the correct time and date.

5. **TRANSMITTER** connector.
   Using the appropriate **TRANSMITTER** connector, connect the test instrument to the 2 Mbit/s receive side of the mux under test.

6. Data Interface connector.
   Using the appropriate data interface connector, connect the INTERCEPTOR 147 to the data circuit under test.

Test Results

1. Watch the **DATA INTERFACE** LEDs to verify that the proper DTE/DCE exchange occurs. Check the **STATUS & ALARMS** LEDs to verify proper detection of signal and pattern.

2. To check circuit continuity, transmit a bit error and verify that it is received (by checking the Bit Errs item in the **LOGIC & TIME** Results category).

3. In the **SUMMARY** Results category, check for the occurrence of any error conditions.

4. In the **LOGIC & TIME** Results category, check the signal lead delay (SL Delay) at the DTE/DCE interface.

5. In the **SIGNAL, CODE & FAS** Results category, check Freq to verify that the receive frequency is at the proper rate.

6. In the **PERFORMANCE** Results category, the G.821 Performance results provide an excellent means of verifying the overall quality of the link under test.

Mux Test Troubleshooting Guide

Symptom:	Likely cause:
No Signal	Verify cabling to mux. Verify the configuration/setup. Check to make sure the CTS/RTS is set to ON.
Pattern Slips	Check the timing configuration on the mux and the INTERCEPTOR 147. Check the receive frequency and Δ PPM.
No Pattern Sync	Verify timeslot mapping. Check signaling lead exchange. Verify data speed in N x 64 kbit/s.
Network alarms	Check receiver termination mode (BRIDGE or MON for data-to-2 M in-service testing). Verify framing configuration.
Bit slips	Check 2 M Rx/Tx timing source. Verify 2 M signal level at Rx/Tx.

Conclusions

Data circuit testing offers significant challenges. Variables, such as signaling leads, modes of timing, and multiple interfaces necessitate that thorough testing of data circuits must be performed prior to system turn-up, and should be part of an on-going network maintenance program.

The TTC INTERCEPTOR 147 provides the features needed by personnel at any support level to test data circuits. In-service and out-of-service testing is made easy, while powerful test features provide the tools necessary to test data circuit problems.

References

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Appendix A: Pin Assignments for Data Interfaces

The TTC INTERCEPTOR 147 Communications Analyzer supports five data interfaces: V.24/RS-232C, V.11/RS-449, V.35, X.21, and codirectional 64 kbit/s. This appendix describes the pin assignments for each interface.

V.24/RS-232C

V.24 CONNECTOR PIN ASSIGNMENTS					
Description:	**CCITT #:**	**Name:**	**Pin:**	**To DTE:**	**To DCE:**
Shield			1		
Tx Data	103	TD	2		→
Rx Data	104	RD	3	←	
Request to Send	105	RTS	4		→
Clear to Send	106	CTS	5	←	
Data Set Ready	107	DSR	6	←	
Signal Ground	102	GROUND	7		
Rx Line Signal Detector	109	RLSD	8	←	
Tx Signal Element Timing, DCE	114	TC	15	←	
Rx Signal Element Timing	115	RC	17	←	
Local Loopback	141	LL	18		→
DTE Ready	108	DTR	20		→
Remote Loopback	140	RL	21		→
Tx Signal Element Timing, DTE	113	XTC	24		→
Test Mode	142	TM	25	←	

X.21

X.21 CONNECTOR PIN ASSIGNMENTS					
Description:	**CCITT #:**	**Name:**	**Pin:**	**To DTE:**	**To DCE:**
Shield			1		
Tx Data	103	T (A)	2		→
Rx Data	104	R (A)	3	←	
Request to Send	105	C (A)	4		→
Clear to Send	106	I (A)	5	←	
Rx Signal Element Timing	116	S (A)	6	←	
Ground	102	G	8		
Tx Data	103	T (S)	9		→
RX Data	104	R (S)	10	←	
Request to Send	105	C (S)	11		→
Clear to Send	106	I (S)	12	←	
Rx Signal Element Timing	116	S (S)	13	←	

V.11/RS-449, V.35, and Codirectional 64 kbit/s

V.11, V.35, G.703 CONNECTOR PIN ASSIGNMENTS							
Description:	**CCITT #:**	**Name:**			**Pin:**	**To DTE:**	**To DCE:**
		V.11	V.35	G.703			
Shield					1		→
ST DCE/DCE SCT (DCE)		ST	SCT		3	←	
Send Data	103	SD	SD		4		→
Send Timing (DCE)	114	ST	TC		5	←	
Receive Data	104	RD	RD		6	←	
Request to Send	105	RS	RS		7		→
Receive Timing (DCE)	115	RT	SCR		8	←	
Clear to Send	106	CS	CS		9	←	
Local Loop	141	LL	LL		10		→
Data Mode	107	DM	DSR		11	←	
Terminal Ready	108	TR	DTR		12		→
Receiver Ready	109	RR	RLSD		13	←	
Remote Loopback	140	RL	RL		14		→
G.703 Transmit (+)				T+	15		
G.703 Transmit (-)				T-	16		
Terminal Timing (DTE)	113	TT	XTC		17		→
G.703 Ground				SGND	19		
ST DCE/DCE SCT (DCE)		ST	SCT		21	←	
Send Data	103	SD	SD		22		→
Send Timing (DCE)	114	ST	SCT		23	←	
Receive Data	104	RD	RD		24	←	
Request to Send	105	RS	RS		25		→
Receive Timing (DCE)	115	RT	SLR		26	←	
Clear to Send	106	CS	CS		27	←	
Data Mode	107	DM	DSR		29	←	
Terminal Ready	108	TR	DTR		30		→
Receiver Ready	109	RR	RLSD		31	←	
G.703 Receive (+)				R+	34		
G.703 Receive (-)				R-	36		
Signal Ground	102	SG	SGND		40		
		RC	SGND		44		
Terminal Timing (DTE)	113	TT	XTC		46		→
Send Common	102A	SC			48		
Test Mode	142	TM	TM		49	←	

Appendix B: Glossary

Async — Asynchronous transmission. A transmission method that sends units of data at the rate of one character at a time, and uses start and stop bits for local timing.

Binary — A system using digits, either 1 or 0, to transmit information.

Bisync — Bisynchronous transmission. A transmission method that sends units of data in blocks.

bit/s — Bits per second. The standard measure of a data transmission rate.

CCITT — Consultative Committee International for Telegraph and Telephony (now called ITU-T). The international advisory committee that recommends worldwide standards for transmission.

Clock — A term for the source(s) of timing signals used in synchronous transmission.

CTS — Clear to Send. A signal from the DCE indicating to the DTE that it may begin transmitting data.

Data — Digitally (expressed as a 1 or 0) represented information; which includes voice, text, facsimile, and video.

DCE — Data Communications Equipment (also known as Data Circuit Terminating Equipment). The equipment responsible for establishing, maintaining, and terminating a data transmission connection.

Delay — The most recently-measured time interval between a stop and start event.

Demultiplex — The process of verifying that data is being received by transmitting a 2 Mbit/s signal and then demultiplexing it on the data side.

DTE — Data Terminal Equipment. The equipment responsible for transmitting data to or from the Data Communications Equipment.

DTR — Data Terminal Ready. A signal sent from a DTE to a DCE, usually announcing that the DTE is ready to transmit data.

EIA — Electronic Industries Association. An organization in the US,consisting of manufacturers of electronics products including data communications equipment. EIA is active in setting interface standards.

End-to-end test	Diagnostic procedure used for transmission equipment.
Handshaking	Exchange of pre-determined signals between two devices establishing a connection.
Interface	A shared boundary, a demarcation point between two devices where the electrical signals, connectors, timing, and handshaking are defined.
kbit/s	Kilobits per second. One thousand bits per second.
LED	Light Emitting Diode. A type of indicator light.
Loopback	Diagnostic test used for transmission equipment; a test message is sent to the device under test, and then sent back through the network to the originator, and compared with the original transmission.
Mbit/s	Megabits per second. One million bits per second.
Modem	Modulator-demodulator, a device used to connect digital data from a transmitting DTE to a signal that can be transmitted over a telephone line.
Multiplexer	A device allowing two or more signals to pass over and simultaneously share a common transmission path.
NTE	Network Termination Equipment.
Polarity	The direction in which current flows.
RS-232C	An EIA recommended standard, this is the most common standard for connecting data processing devices.
RTS	Request to Send. A signal sent from the DTE to the DCE, informing the DCE that there is data to send.
Sync	Synchronous transmission. Transmission method in which data bits are sent at a fixed rate, with the transmitter and receiver synchronized.
ST	Send Timing originates from a DCE.
TT	Terminal Timing originates from a DTE.
V.35	A CCITT wideband interface recommendation. Typically used in applications which require a balanced, high-speed data interface.