Design of 0.35µ Analog CMOS Amplifier for EEG Signals Amplification

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ABSTRACT

The thesis is about amplification required for the Electroencephalogram signals commonly referred to as EEG signals, which are the signals recorded in the human brain. Hence they contain information about the brain activities. However there are concerns in retrieving the information from these EEG signals. The first and foremost concern is the small signal amplitude of the EEG signals. This forces a requirement to provide an amplifier.

The next concern in measuring the EEG signals is the design of an amplifier. There are many challenges in designing the amplifier like the power and area. This thesis will discuss the design of such an amplifier that has high gain, high CMRR and relatively low power and more importantly amplifying the low amplitude EEG signals.

List of Headings:

List of Figures:

List of Tables:

CHAPTER-1

INTRODUCTION

INTRODUCTION:

This chapter produces a brief introduction about what this thesis and project is about. Starting with the introduction about the bio potential signals, this chapter continues with more detail on EEG signals, its spectrum and other characteristics like about how they are processed with relevant Figures and references wherever necessary for better understanding.

1.1 INTRODUCTION TO BIO POTENTIAL SIGNALS:

The human body is made of cells. Each cell produces electrical activity by the ion exchange process[1]. The K^+ and Na^+ are the two types of ions that are produced by our cells. An electric potential is produced by the difference in ionic potential between these two ions. Two kinds of potentials can be produced by the cells. They are the action potential and the resting potential. If the concentration of Na+ ions outside the membrane is higher than the concentration of K+ ions inside the membrane then the potential caused is called resting potential. Similarly, if the concentration of the K+ ions outside the membrane is higher than the concentration of the Na+ ions inside the membrane then the potential produced is called action potential. It is found that the resting potential can produce a potential of -70mV and the action potential can produce the potential of +40mV [2]. This process keeps going on a cycle. Hence by this process the cells in our body, produces a varying voltage. Three main signals are derived from this voltage. They are the ECG, EMG and EEG.

The ECG signals are referred to as Electro Cardiogram signals. These signals are used to calculate the electrical activity of the human heart [3]. The EMG signals are called Electromyography signals. These are the signals produced by the contraction of muscles in our body. Finally, the EEG signals are called Electroencephalogram signals. These signals

are produced in the brain. These are the three main bio potential signals in our body. However, this thesis will be focused only on the EEG signals apart from the other two.

1.2 EEG SIGNALS:

The Electroencephalogram signals are used to measure the electrical activity of the human brain. These signals are of very low power in the order of μV and also operate in low frequencies [4].

Each neuron in our brain carries some amount of information and some amount of noise. A single neuron cannot reproduce the information. Hence we cannot retrieve any information from a single neuron, since it is off very low value. So, at some points in brain, millions and millions of neuron meet each other and exchange their information. Hence the available information at certain points in brain, where these neurons meet also increases. Thus at those points we can have a better information and comparatively higher voltage. These points are called neural field potentials. Hence at these points the EEG signals of our brain are measured [5]. Figure-1 [6], produces the detailed picture of this process.

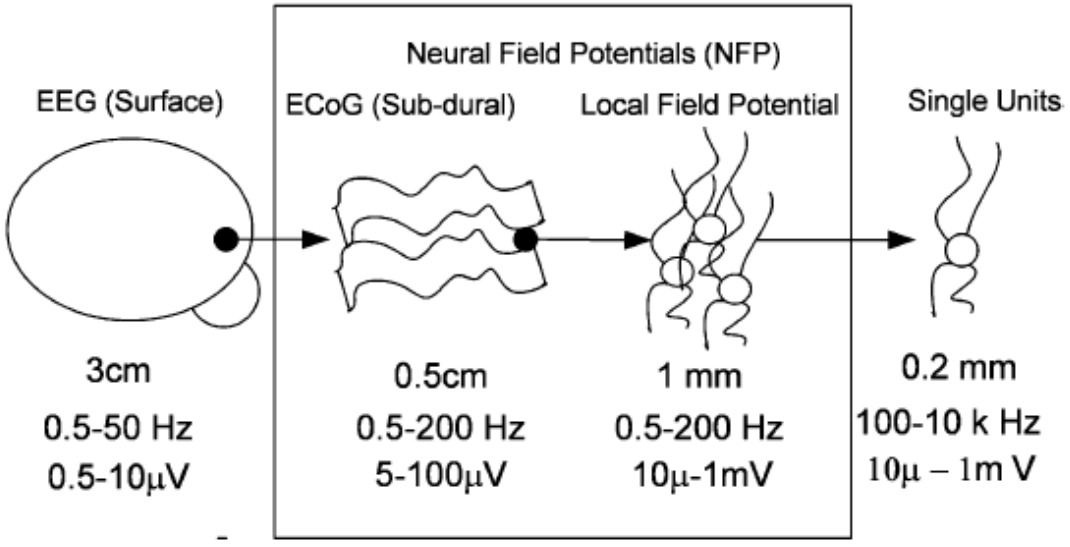

Figure-1: EEG signals[6]

The EEG signals from our brain can be measured by placing electrodes at those points(NFP). Different voltages are produced at various points around the skull. Nearly 25-

30 electrodes are placed all over the skull in order to measure the EEG signals. Figure-2 [7] shows the spectrum of the bio potential signals. From the spectrum we can see that the EEG signals are of very low voltage. Hence with this very low voltage signal we cannot get any information. So we need an amplifier to amplify this small voltage signals from the electrodes placed around the skull.

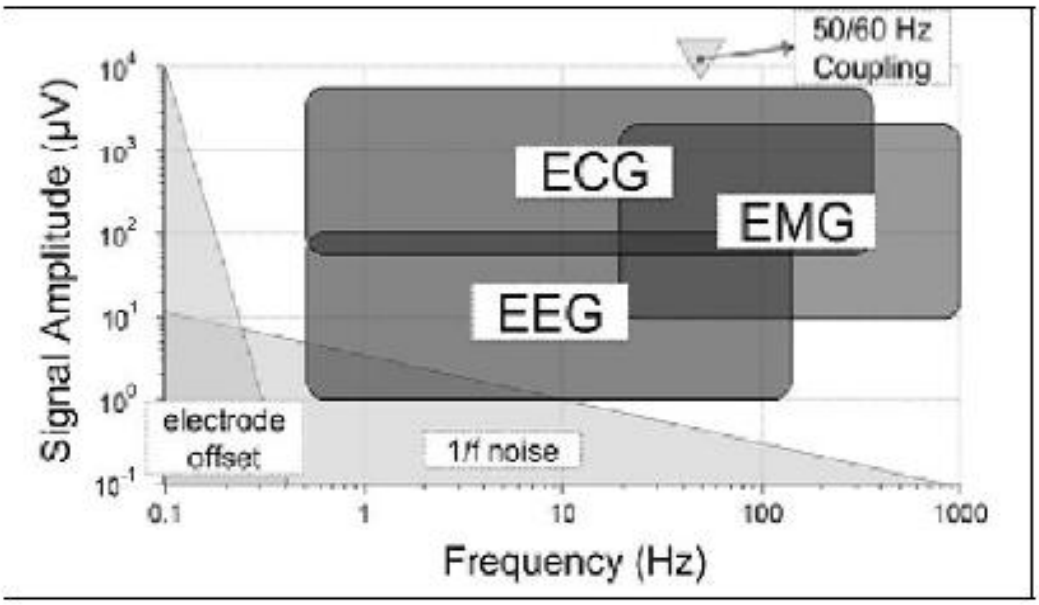

Figure-2: Spectrum of the Bio potential signals[7]

1.3 EEG SIGNAL PROCESSING:

The above section illustrated the need for an amplifier. This section will be focused on how the EEG signal is processed thoroughly. Starting with the need for an amplifier, as said earlier, the amplifier is required to amplify the low voltage EEG signals. The EEG amplifiers convert the weak signals from the brain into a more informative signal for the output device [8]. These are the differential amplifiers that are useful when measuring the relatively low level signals. In some designs, the amplifiers are the set up of a pair of electrodes that detects the electrical signal from our brain [8]. The electrode signals are then transferred to the amplifier through wires and the amplifier stabilizes the signals and amplifies it by certain amount. The amplifier translates the different incoming signals and cancels the one that are identical [8]. Therefore the amplified signal is the differentially

picked signals from the electrodes. The stabilized and amplified EEG signals is then further processed if higher efficient signals are required and then produced onto an Analog to Digital converter. This digitized signal is then produced on to the Signal processor. The processed signal can then be retrieved using suitable mechanisms to produce the output. The detailed operation of this process is produced in Figure-3 [6].

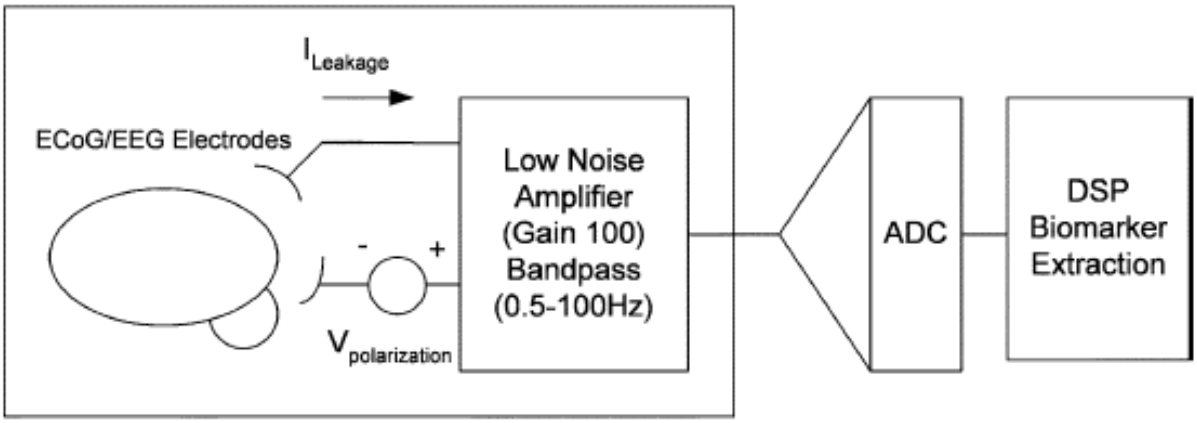

Figure-3: EEG signal processing mechanism[6]

Thus a brief description on the EEG signals and its characteristics is produced in this chapter. The thesis will now focus on the design of amplifier. Chapter-2 produces the brief outline about the constraints and challenges in designing the amplifier and also about the different methods in which an amplifier can be design. Chapter-3, Chapter-4 gives a detail study about the amplifier design, designed in this project and chapter-5 gives a conclusion on this project and the thesis.

CHAPTER -2

CHALLENGES IN DESIGNING AN AMPLIFIER

This chapter provides brief details on the design challenges of an amplifier. The first part in this chapter is about the challenges in designing the amplifier and the second part is about the requirements for designing the amplifier for the bio potential signals.

2.1 CHALENGES IN DESIGNING AN AMPLIFIER:

The first and foremost challenge in designing an amplifier is the noise factor. The amplifier that is to be designed must combat noise. From Figure-2, which depicts the spectrum of the bio potential, we can find that all these signals exist at very low frequency. Since these signals exist at very low frequency of operation they produce some noise. Also as said earlier, the neural field potential also produces noise. Hence we must design an amplifier that can combat these noise sources. The noise that is of more concern in this amplifier is the flicker noise.

2.2 FLICKER NOISE:

In 1918 William Schottky predicted the occurrence of the frequency independent white noise. Later in 1925 J.B.Johnson successfully measured it and found it as the “flicker noise” at low frequency [9]. Figure-4 [10] shows the occurrence of the flicker noise in electronic device.

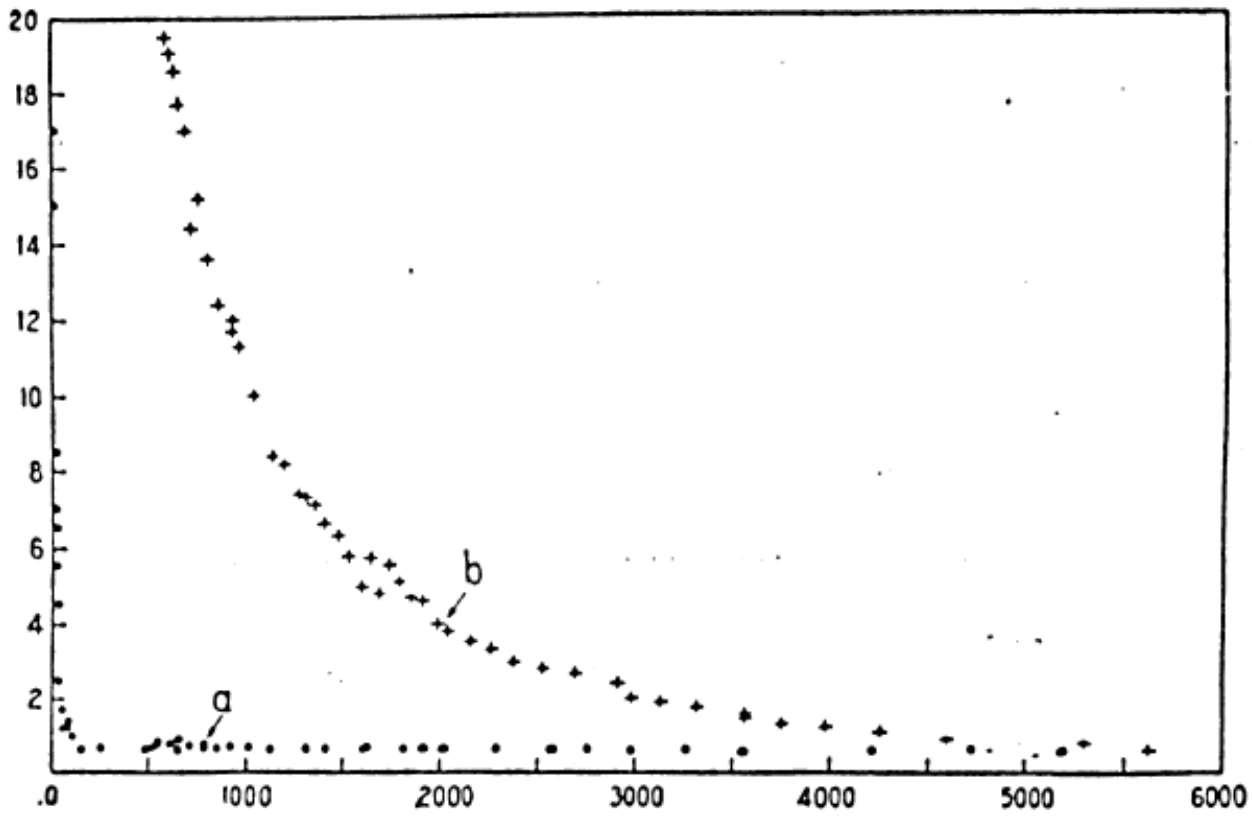

Figure-4: Occurrence of flicker noise in electronic devices[10]

Units: X axis- Frequency

Y axis- Amplitude

The flicker (1/f) noise in metal oxide field effect transistors (MOSFET) has been studied over decades. Though it has been studied over decades, the clear picture of the noise generation is yet to be found and is believed to be due to current fluctuations [11].

As discussed earlier, due to low frequency of operation of the bio potential signals, noise is of main concern. This low frequency of operation produces a noise called flicker noise [6]. The main character of the flicker noise is that, the noise increases as the frequency of operation decreases. Hence as the frequency decreases the noise increases.

The flicker noise is also called as 1/f noise meaning the noise increases as the frequency decreases. It is also called as the pink noise as it occurs in the pink spectrum. It is believed

that the flicker noise occurs in almost all electronic devices [12]. Figure-5 [13] shows the graphical representation of the flicker noise.

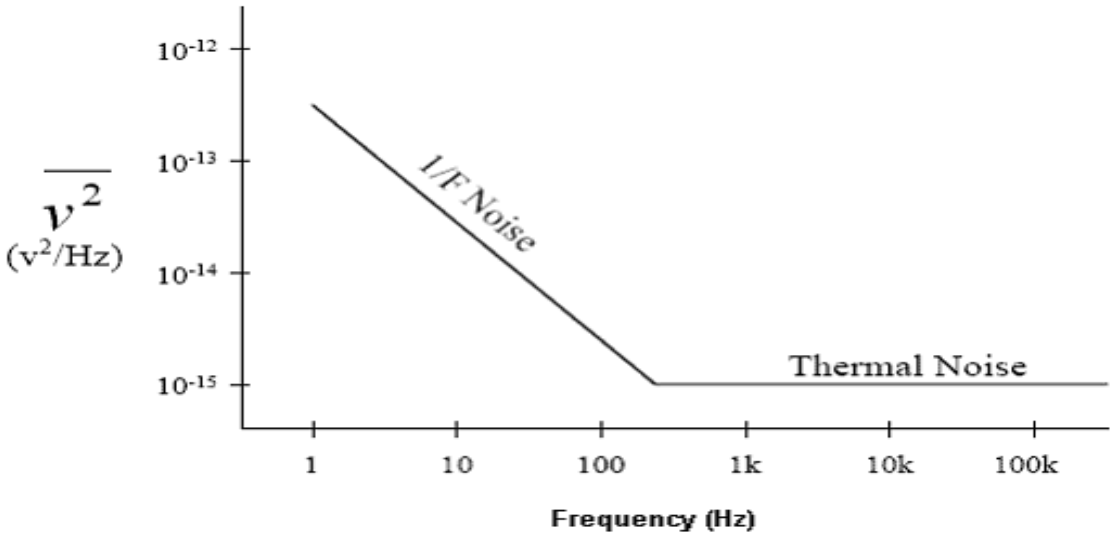

Figure-5: Graphical representation of flicker noise[13]

The above Figure shows the characteristic of the flicker noise. From the above Figure, it is clearly seen that the flicker noise is high at low frequencies. As the frequency of operation increases, the flicker noise decreases and at a certain point, the flicker noise turns into a thermal noise. The frequency at which the flicker noise turns into the thermal noise is called corner frequency.

The flicker noise is believed to occur due to random movement of charges in the gate oxide and substrate interface. Since the charge carriers move randomly, they are trapped and released randomly thereby producing the flicker noise [14]. The flicker noise is given by the equations 1 and 2,[14]

$$V_n^2 = \frac{K}{C_{ox}WL\ f} \qquad \text{Equation (1)}$$

$$V_n = \frac{K}{\sqrt{f}} \qquad \text{Equation (2)}$$

K is the process dependent constant. W is the width of the transistor and L is the length of the transistor. From the above equation it is clear that the power spectral density is inversely proportional to the frequency, hence as the frequency decreases the noise increases. From the above equation it is also seen that the flicker noise is inversely proportional the width and length of the transistor. Hence increasing the width and length of the transistor will provide us a decrease in flicker noise.

As mentioned earlier, the flicker noise is due to trapping and releasing of the charge carriers in the gate oxide and silicon interface. Thus the flicker noise is found a bit higher in NMOS when compared with PMOS as electrons are the main charge carriers in the NMOS. In PMOS, since holes are the majority charge carriers, the flicker noise is comparatively low in PMOS. Hence it is better to use the PMOS input device for better flicker noise performance.

2.3 METHODS TO REDUCE THE FLICKER NOISE:

The last section provides a brief description on the flicker noise formation and its effects. This section will provide a detailed explanation on the methods to avoid the flicker noise formation. One such popular method in limiting the flicker noise in the electronic devices is the chopper method. The amplifier which uses this chopper technique is referred to as Chopper Amplifier.

2.4 CHOPPER AMPLIFIER:

The term chopper in electronics is defined as a switch that used to interrupt one signal under the control of another [15]. The first chopper stabilized amplifier was designed in 1949 by Edwin.A.GoldBerg. This set-up uses a normal op-amp with an additional AC amplifier that goes alongside the op-amp. The chopper gets an AC signal from DC by switching between the DC voltage and ground at a fast rate (60Hz or 400Hz). This signal is then amplified, rectified, filtered and fed into the op-amp's non-inverting input. This vastly improved the gain of the op-amp while significantly reducing the output drift and DC offset [16].

Chopper amplifiers are best for lowest offset and drift performance [17]. In addition to the techniques by which the flicker noise can be reduced that were like increasing the aspect ratio of the transistor that is increasing the width and length of the transistor and using PMOS input devices, if we use this chopper technique then the amplifier will produce better immunity to the flicker noise. There are few designs by which a chopper amplifier can be designed. Let us briefly discuss about them in detail in next section.

2.5 CLASSICAL CHOPPER AMPLIFIER:

Of the many methods of designing the chopper amplifier, we are about to discuss the classical chopper amplifier method first. This amplifier is also known as the Auto Zero chopper stabilized amplifier. The Figure-6 [18] shows the auto zero chopper stabilized amplifier method.

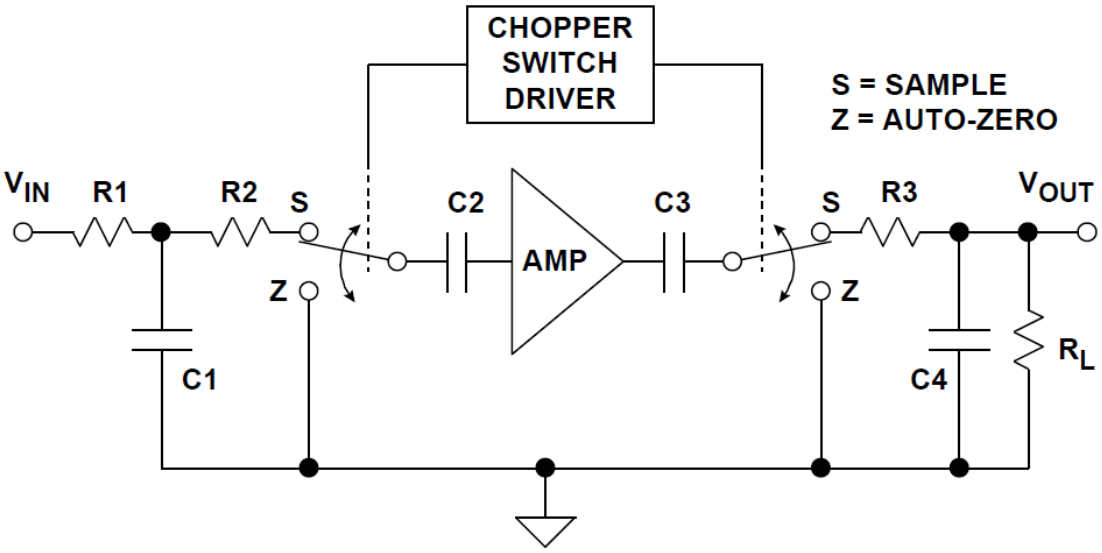

Figure-6: Classical Chopper Amplifier[18]

The above Figure gives a picture of the classical auto zero chopper amplifier. This amplifier has two switches S and Z. Switch S is to sample and switch Z is called auto zero. When the amplifier is thrown to switch Z, the capacitors C2 and C3 gets charged. Now when the switch is thrown to S position, the circuit is closed and v_{IN} is connected to v_{OUT} through the path R2,C2,C3 and R3. The sampling frequency is usually chosen higher. Thus

by this prolonged switching activity, the signal is sampled and chopped thereby reducing the flicker noise occurrence in the circuit.

The resistor R1 and capacitor C1 acts as an anti aliasing filter [17] thereby preventing the aliasing effect of the signals. The load resistor R_L and capacitor C4 is chosen so as to get the desired output. This method of chopper amplifier is called auto zero chopper stabilized amplifier. This is a classical method for the chopper amplifier.

2.6 CORRELATED DOUBLE SAMPLING METHOD:

An advancement to the auto zero classical chopper stabilized amplifier is called correlated double sampling method. Figure-7 [18] shows the picture of a correlated double sampling method of chopper stabilization.

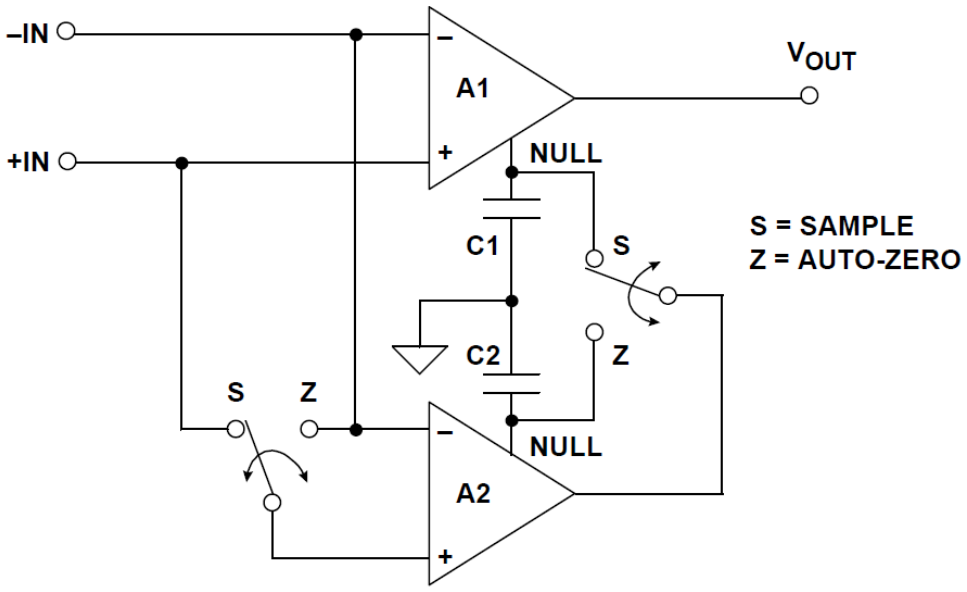

Figure-7: Correlated Double Sampling method[18]

The above Figure shows the double sampling chopper stabilization method. When compared with the auto zero technique this technique uses two amplifiers, amplifier A1 and amplifier A2.

The amplifier A1 is the main amplifier and amplifier A2 is called as the nulling amplifier [18]. The amplifier A2 turns on when the amplifier A1 has an offset voltage. If the

amplifier A1 has an offset voltage then, the amplifier A1 is detached from amplifier A2. Now the amplifier A2 turns on and hence it will prevent the offset being driven to the output. To drive the offset of amplifier A1, the amplifier A2 must not be driven by the offset voltage. To overcome this problem, we have a zero switch. If the amplifier A2 is about to enter into the offset voltage then it turns on the switch to zero there by it detaches itself from being driving the offset voltage.

During the auto zero mode the correction voltage for amplifier A1 is held by the capacitor C1 and similarly, the correction voltage for the amplifier A2 is held by the capacitor C2 [18]. Here the input is connected to the output through the amplifier A1 only. Hence it is necessary to define exact bandwidth parameter to this amplifier A1 in order to get the required output. The amplifier is normally provided with a higher sampling frequency. The frequent switching activity of the amplifiers causes the effect of chopping, thereby reducing the flicker noise in the output signal.

2.7 OPEN LOOP CHOPPER STABILIZED AMPLIFIER:

The other popular and most widely used chopper stabilization method is the open loop chopper stabilization technique. In this technique the amplifier is modulated to higher frequency, amplified and then demodulated back after proper amplification. The Figure -8 [19] shows the diagram of an open loop chopper stabilization amplifier.

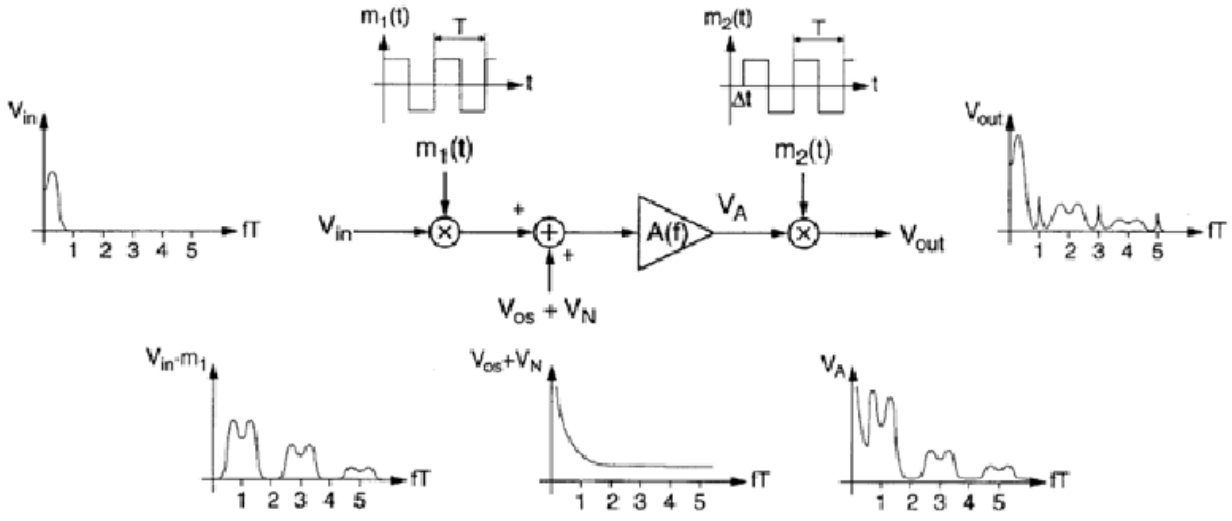

Figure-8: Open loop Chopper Stabilization Technique[19]

The above Figure shows the open loop chopper stabilization technique. In the Figure, Vin is the input signal to the amplifier. M1(t) is the modulated signal. VOS is the offset voltage and VN is the noise voltage. A(f) is the amplifier, VA is the amplified signal and m2 (t) is the demodulated signal.

Here the input signal is first up modulated to higher frequency using an AC carrier where there is no flicker noise. Note that the modulation frequency must be so high such that there is no flicker noise in that frequency of operation. The offset and noise voltage is then added to this AC modulated signal. The signal is then passed through an amplifier.

The amplified signal is then demodulated back to the normal frequency of operation. Thus the demodulated signal from the de modulator will be free of the flicker noise. This signal is then pass through the low pass filter in order to retrieve the signal at the output.

As shown, the modulated signal is the product of the given input signal and the AC carrier signal. The frequency spectrum of this multiplied signal is shown in Figure-8. From this Figure, it is clear that this multiplied signal is transposed to the odd harmonic frequencies. Later, this signal is amplified by the amplifier. This amplified signal is then demodulated back to its own frequency of operation by the demodulator signal m2 (t).

In order to recover the original signal, the demodulated signal is provided to a low pass filter. The cut off frequency of this low pass filter must be atleast half the chopping frequency for which the signal is modulated before. Hence the output signal from this low pass filter will be free of the flicker noise.

The noise and offset in the amplifier is added only once. After amplification, the noise and the offset is transferred to the odd harmonics. This odd harmonic signal is then removed by the low pass filter leaving behind the original signal in the even harmonics. The signal is then retrieved easily. Thus the noise and offset are removed by the amplifier and by this method.

2.8 CLOSED LOOP CHOPPER AMPLIFIER:

The last section gave us an explanation on the open loop method of chopper amplifier. This section will provide us a detail on the architecture of a closed loop chopper amplifier. Figure -9 [6] provides this design.

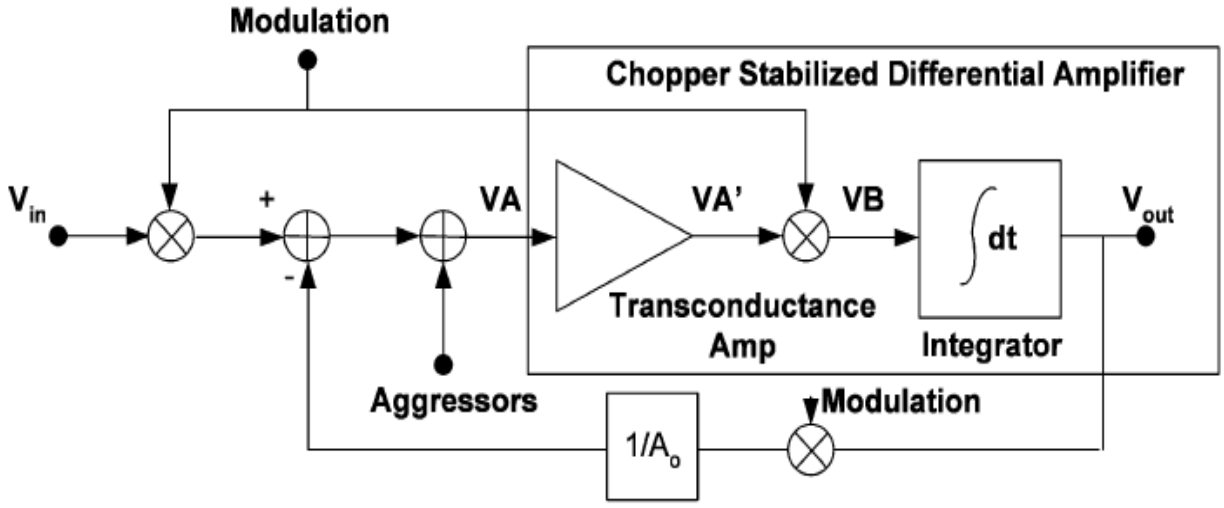

Figure-9: Closed loop Chopper Amplifier[6]

The above Figure shows a picture of the closed loop chopper amplifier. Here we could find that the output is fed back to the input for better performance. The distortion produced in the amplifier will be reduced by this method. The gain of the amplifier will be increased by this method. The power dissipation also will be reduced by this closed loop chopper amplifier [6]. The output signal will be free of flicker noise. When this signal is fed back to the input, this signal will be modulated and amplified again. Hence by repeating this process, we will get better output signal and also with high gain.

2.9 DISADVANTAGES OF CHOPPER AMPLIFIER:

Though chopper amplifier helps in eliminating the flicker noise and offset, it also has some disadvantages. One of the main drawbacks of this chopper method is found to be its complexity. Starting from the classical chopper amplifier to the closed loop chopper amplifier, we could find its difficulty in its complex structure. Moreover the chopper amplifier needs a constant monitoring in order to ensure that there is no flicker noise presence in the signal [19].

Thus this chapter provided us a clear picture on the challenges that are to be faced in the design of the amplifier. We also had a look on the methods that can combat the noise in the design of an amplifier. Keeping this in mind the next chapter will provide us an approach on the requirements and specification for the amplifier design. The next chapter is the first step for our amplifier design.

CHAPTER-3

REQUIREMENTS AND SPECIFICATON FOR THE AMPLIFIER DESIGN

An amplifier design must have some requirements like what we need from our amplifier output and how we want our amplifier to respond us for a given input. This chapter will deal about the desired requirements for the amplifier design. The following parameters to be discussed are the important requirements for the amplifier design to be fulfilled.

3.1 GAIN OF THE AMPLIFIER:

This is the most important and foremost amplifier requirement. The amplifier gain will gives a detail about the efficiency of our amplifier designed. The gain of the amplifier is usually defined as the ratio of the output voltage to the input voltage. The gain of the amplifier provides a detail on how far the signal has been strengthened [20]. Gain of an amplifier gives us an estimate on the power of an amplifier.

The gain of an amplifier can be expressed generally as in Equation 3.

$$Gain = \left(\frac{Vout}{Vin}\right) \qquad \text{Equation (3)}$$

Or in reference to the 20dB log scale, the gain of the circuit can be expressed as,

$$Gain = 20\log\left(\frac{Vout}{Vin}\right)\text{dB} \qquad \text{Equation (4)}$$

Hence the gain of an amplifier is a most important parameter. As mentioned earlier, the gain of the amplifier must be high. The gain of an amplifier can be increased by increasing the ratio of the output voltage to the input voltage. From the above two equations we can see that the gain is directly proportional to the output voltage and inversely proportional to the input voltage. Hence higher the output voltage and lesser the input voltage, higher will be the gain of an amplifier.

3.2 CMRR:

CMRR is an acronym for Common Mode Rejection Ratio. A differential amplifier uses a differential signals to amplify the signal. The main use of the differential amplifier is that since we use the differential signals, the error and noise occurrence during the amplification

of the signal will be low. Although we use differential signal, there will be still some common mode signals that are common to both these differential signals. Hence we must remove that common mode signal that is common to both these differential signals. This process of limiting this common mode signal is called Common Mode Rejection Ratio (CMRR). A differential amplifier must have high CMRR so that it can keep the common mode signal as low as possible. Higher CMRR increases the efficiency of the amplifier. Figure-10 could explain this process.

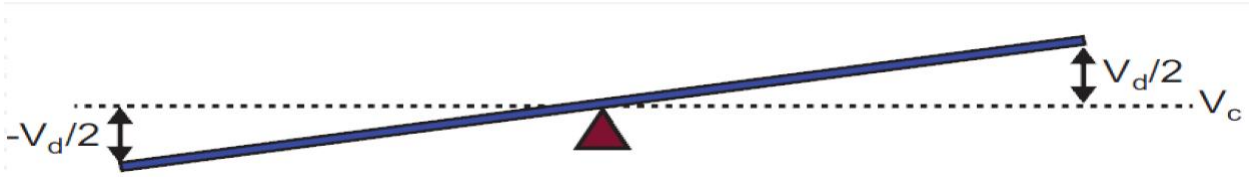

Figure-10: Common mode and Differential signals

Figure[10] shows the common mode signal and differential signals. The V_C is the common mode signal. V_d is the differential signal. Since we use the differential signal this differential signal V_d is split into two halves $+V_d/2$ and $-V_d/2$. We can see that this differential signal swings around this common mode signal. Hence both these differential signal has some common mode signal that is common to them. Thus this common mode signal must be kept as low as possible to provide better output.

If Vi1 and Vi2 are the two inputs of a differential amplifier, then the differential signals can be given by the following equation

$V_{id}=Vi1-Vi2$ Equation (6)

Similarly the Common mode signal can be given by the following equation

$V_{ic}=\frac{Vi1+Vi2}{2}$ Equation (7)

From the above two equations we can find the two inputs of the differential amplifier. This input signal can be represented by the following equations

$$Vi1=V_{ic}+\frac{Vid}{2}$$ Equation (8)

Similarly the other input can be given by

$$Vi2=V_{ic}-\frac{Vid}{2}$$ Equation (9)

Figure-11 shows an op amp with two inputs Vi1 and Vi2. Figure-12 [21] give us a picture of an operational amplifier with the differential and common mode signals. From Figure-11 we can find that the common mode signal is the input signal that is common to both these differential inputs. The input that appears equally to this Vi1 and Vi2 is called the differential input.

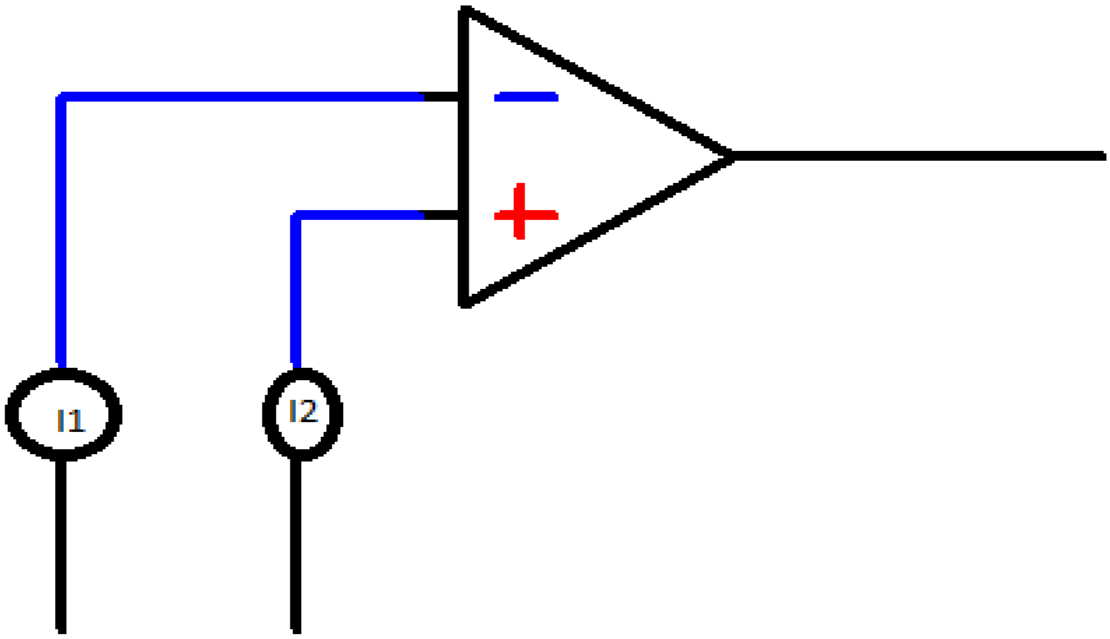

Figure-11: Operational Amplifier with two inputs i1 and i2

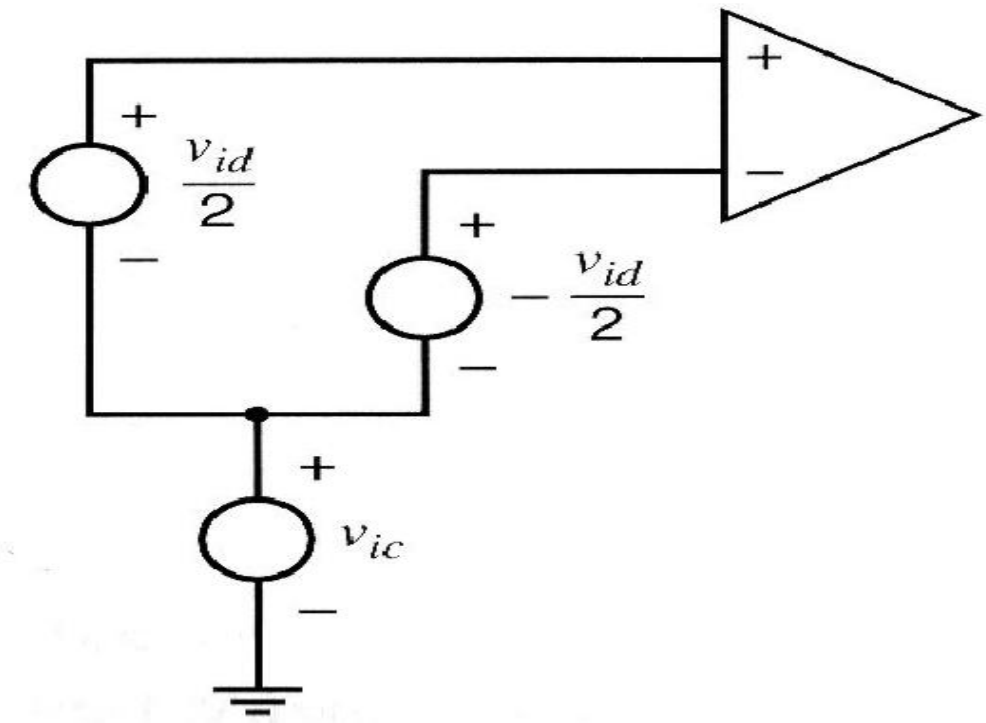

Figure-12: Operational Amplifier with Differential Signal and Common mode Signal

Similar to the input variables we can also define the output variable. The differential output is given by

$V_{OD}=V_o1-V_o2$ Equation (10)

The common mode output is given by

$V_{OC}=\frac{Vo1+Vo2}{2}$ Equation (11)

The common mode output is also called as the average output.

From equation (10) and equation (11), we can derive the output as

$Vo1=V_{OC}+\frac{VOD}{2}$ Equation (12)

$Vo2=V_{OC}-\frac{VOD}{2}$ Equation (13)

We can define the differential and common mode output signals as

$VOD = A_{dm} V_{id} + A_{cm\text{-}dm} V_{ic}$ Equation (14)

$VOC = A_{dm\text{-}cm} V_{id} + A_{cm} V_{ic}$ Equation (15)

Where,

A_{dm} is the Differential mode Gain is the change in differential output to the change in differential input and can be denoted by

$$A_{dm} = \frac{Vod}{Vid}$$ Equation (16)

$A_{cm\text{-}dm}$ is the Common mode to Differential mode Gain and is defined as the ratio of change in differential output to the change in common mode input and is given by

$$A_{cm\text{-}dm} = \frac{VOD}{Vic}$$ Equation (17)

$A_{dm\text{-}cm}$ is the Differential mode to Common mode Gain and is defined as the ratio of change in the Common mode output to the differential input

$$A_{dm\text{-}cm} = \frac{VOC}{Vid}$$ Equation (18)

A_{cm} is the Common mode Gain and is defined as the ratio of change in Common mode output to the input common mode signal

$$A_{cm} = \frac{VOD}{Vic}$$ Equation (19)

As mentioned earlier the differential amplifier is to amplify the differential signal and must reject the common mode signal. The output signal must be proportional to the input signal. Change in input differential signal should produce a change in output signal and variation of the common mode signal must be rejected. Therefore the differential gain A_{dm} must be higher than all the other gains as mentioned earlier. With perfectly balanced conditions, equations (17) and (18) can be zero. But even in that balanced condition (16) and (19) cannot be zero. This gives rice to the new definition called CMRR. Thus CMRR can be represented as equation 20.

$$CMRR = \frac{Adm}{Acm}$$ Equation (20)

Thus CMRR is defined as the ratio of the Differential mode Gain to the Common mode Gain. Thus from this equation it is clear that with higher CMRR,the Common mode gain will be reduced. Hence the amplifier that we design must have a higher CMRR.

3.3 OFFSET:

Since Operational Amplifiers works in DC, they have DC operating problems. One such problem is called the Offset Voltage. This can be explained as follows. If the both inputs of the op amp is connected to the ground, we can find that there is still some output voltage exists rather than being zero. This is called output offset voltage of an op amp.

Similar to this output offset voltage, there exists input offset voltage which arises due to the unavoidable mismatches due to the input differential stage in the op amp [22]. Figure-13 shows the diagram of an op amp whose inputs are tied to ground.

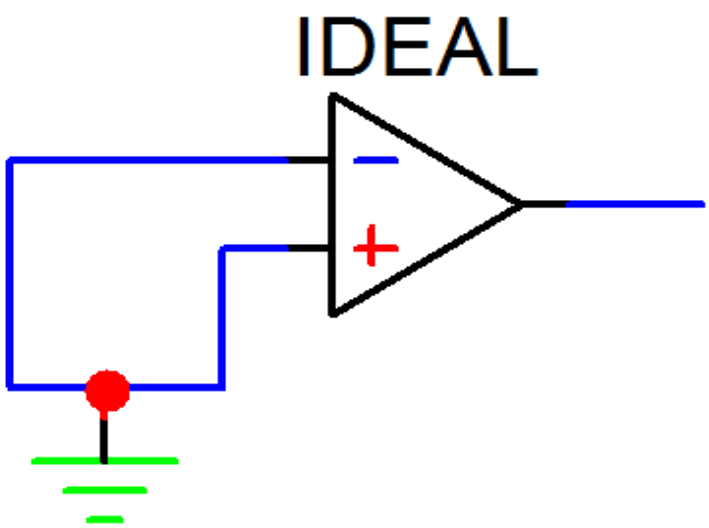

Figure-13: Op amp input tied to ground

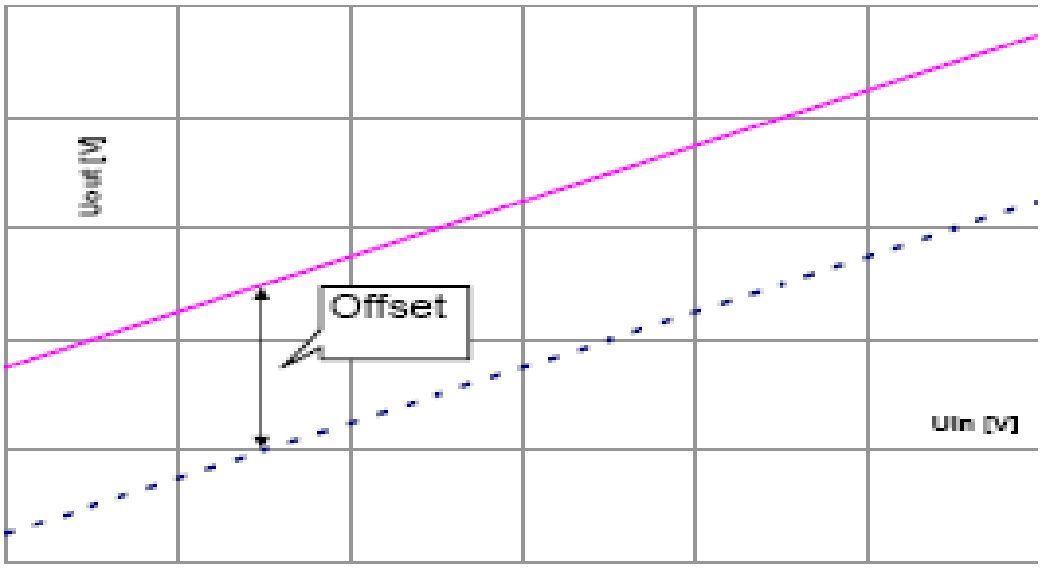

Figure-14: Output Offset Voltage of an Opamp[24]

Figure 14, shows the output offset voltage. It seen that the actual output should be the blue doted lines which passes through the origin. But due to the offset error the output that is produced is the pink color straight line. Thus the output that is produced when the inputs are tied deviates from the actual output. This is called as an offset voltage.

3.4 SLEW RATE:

Slew rate of an op amp is defined the change in output voltage with respect to the time. Its unit is V/µs. It can be given by,

$$\text{Slew Rate} = \frac{dvo}{dt} \qquad \text{Equation (21)}$$

Thus slew rate can be defined by the rate of change in the output with respect to the input signal. Normally in an op amp the output follows the input. But if we expect the output to respond faster to the given input, then slew rate comes into play. The output can respond faster to the input only after a certain limit. To that limit, the output will ramp towards the actual output.

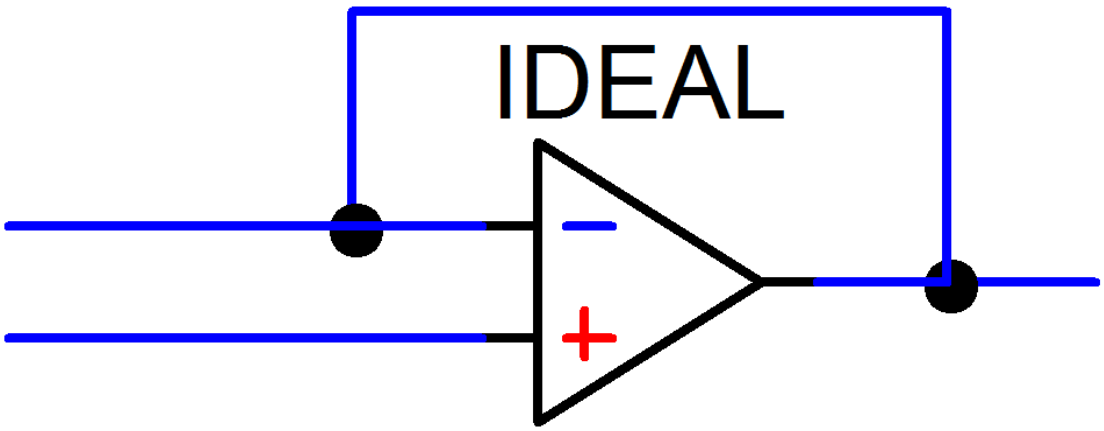

Figure-15: An ideal op amp

The above Figure shows an ideal op amp. The output of the op amp is fed back into one of its input.

The slew rate can be given by the formula

Slew rate = $2\pi f(V_{PK})$ Equation (22)

Where

V_{PK} is the peak amplitude of the amplifier

f is the frequency of operation

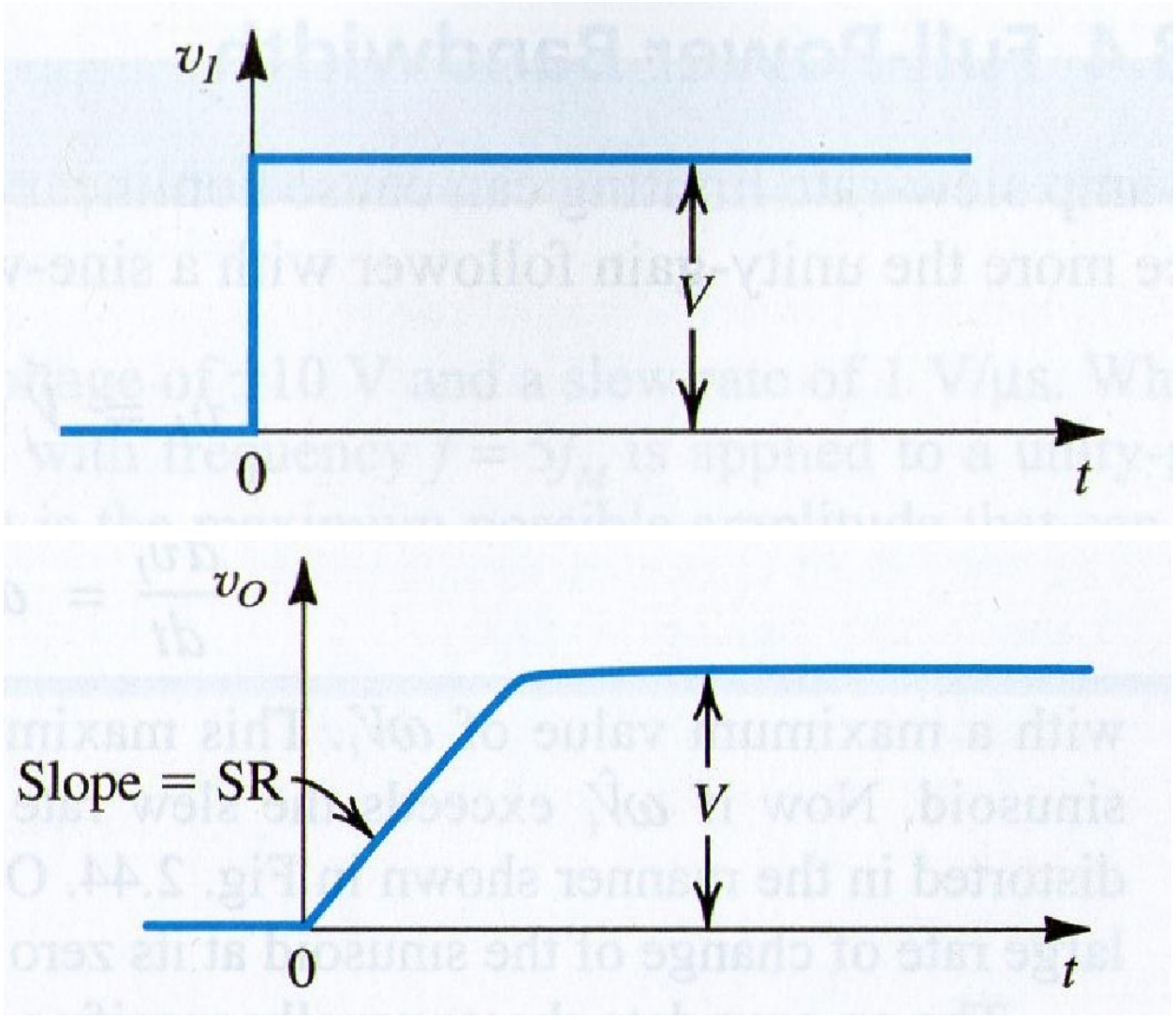

Figure-17: Output Response of the ideal Op amp[22]

Figure-16 and Figure-17 [22] shows the input and output response of the ideal Op amp shown in Figure-14. From Figure-15 we can see that the input of an Op amp was a simple pulse signal. But the output response of the amplifier from Figure-16 we find that the output takes some time to reach its maximum value. After that it remains constant. This slope that makes the output to reach its actual value is called Slew Rate. The slew rate cause a non linear distortion of the input signal such that when its amplitude and frequency would require V_O to change greater than the measured slew rate.

3.5 OTHER FACTORS:

The other factors that concern the design of an op amp is the power and current consumption. It should be noted that the amplifier we designed must consume less power and current in order to produce better output.

3.6 COMPLETE REQUIREMENTS FOR THE AMPLIFIER DESIGN:

The below table shows a set of requirements that is provided by the International Federation of Clinical Neurophysiology Standards based on the AMS 0.35u technology process which is a good reference for this project.

SPECIFICATIONS	**VALUE**
Technology	AMS 0.35µ
Power Supply	3.3 V
Gain	75 dB
CMRR	100dB
Power Dissipation	100µW

Table 1 : Requirements of the amplifier design

3.7 AMS 0.35µ TECHNOLOGY

The amplifier to be designed in this project is using the AMS 0.35µ technology. AMS stands for Austrian Micro Systems. The term 0.35µ shows the minimum length of a transistor that will be used in this design. The software that is to be used in this project is the CADENCE. This design technology has a separate library. Every device we use in this technology like the PMOS and the NMOS devices have their own design parameters like the threshold value. So it is necessary to study the parameters of these MOS devices in this technology so that it will be useful for our amplifier design to proceed further. A further important factor in this technology is to study about the supply voltage that is necessary for this technology. The supply voltage for this technology is generally chosen to be 3.3 V. So we will be using the same power supply voltage throughout this amplifier design

3.8 PMOS CHARACTERISTICS OF 0.35µ AMS TECHNOLOGY:

A MOS device has four terminals. The source, drain, gate and body. Proper connection must be made to all these four terminals in order to make the transistor work. Though both PMOS and NMOS has the same three terminals, there are a few similarities and differences between the connection of these terminals in both these transistors. For both the transistors, the gate terminal acts as the input terminal. In order to make the transistor work, a proper input voltage must be provided to this gate terminal. The input must be chosen in such a way that the transistor is ON. Similar to the gate terminal that acts as the input, the output is produced at the drain terminal.

For a PMOS, the source terminal and the body terminal must be connected to the power supply. Figure-18 shows this connection of the PMOS device in cadence. We could find from the Figure that the source of the PMOS device is connected to the power supply of 3.3 V as said before. A constant supply voltage is provided to the gate terminal in order to make the transistor work.

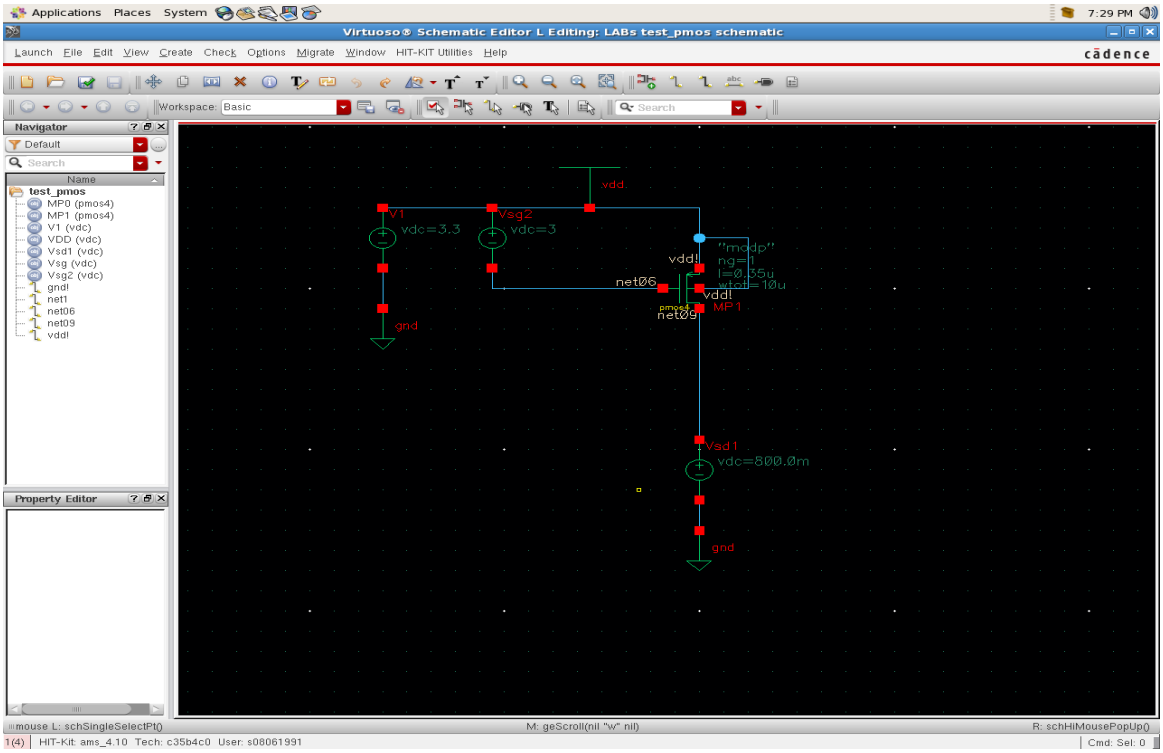

Figure-18:PMOS schematic

Now after creating the schematic, we need to simulate this schematic in order to measure the threshold voltage from our output displayed. So on simulating the gate source voltage vs the drain current we get the following result. The result of the schematic is shown in Figure-19.

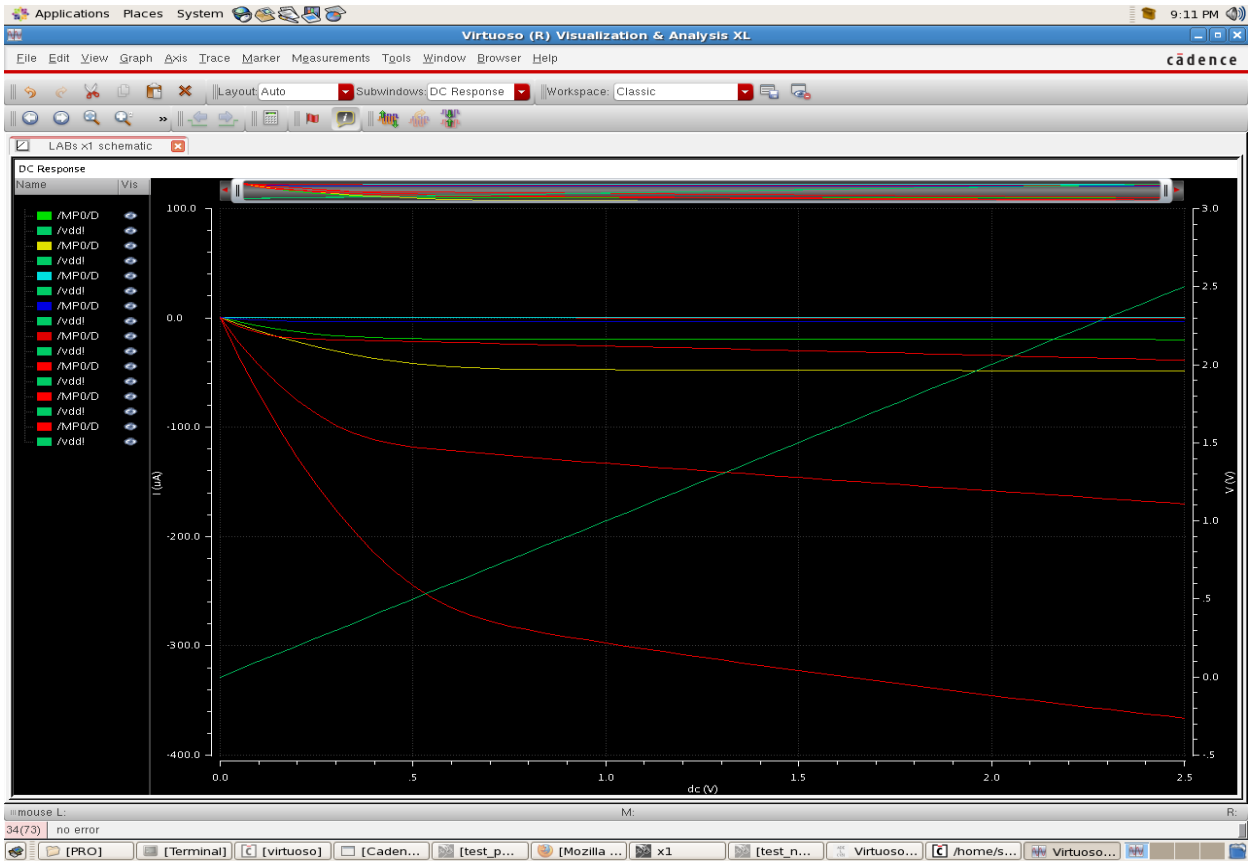

Figure-19: Simulation result of the PMOS.

The above Figure-19 shows the simulation result of our PMOS device designed in our schematic. The above Figure is a graph between the gate source voltage vs the drain current(Id). The test is performed with the various gate source voltages(Vgs) so that we can note the changes in the drain current of the transistors. Thus the test is performed with five different Vgs voltages. From this simulated result, we can find the threshold voltage by noting the voltage at which the transistor is ON. Thus from the above result, we can measure the threshold voltage of the PMOS device as 0.7 V.

3.9 NMOS CHARACTERISTICS OF THE AMS 0.35µ TECHNOLOGY:

Similar to the PMOS characteristics, we need to find the characteristics of the NMOS device. Like the source of the PMOS is connected to the power supply, the source and body of the NMOS device must be connected to the ground in order to make the transistor work.

The schematic design of the NMOS we designed in the cadence is shown in Figure-19 below.

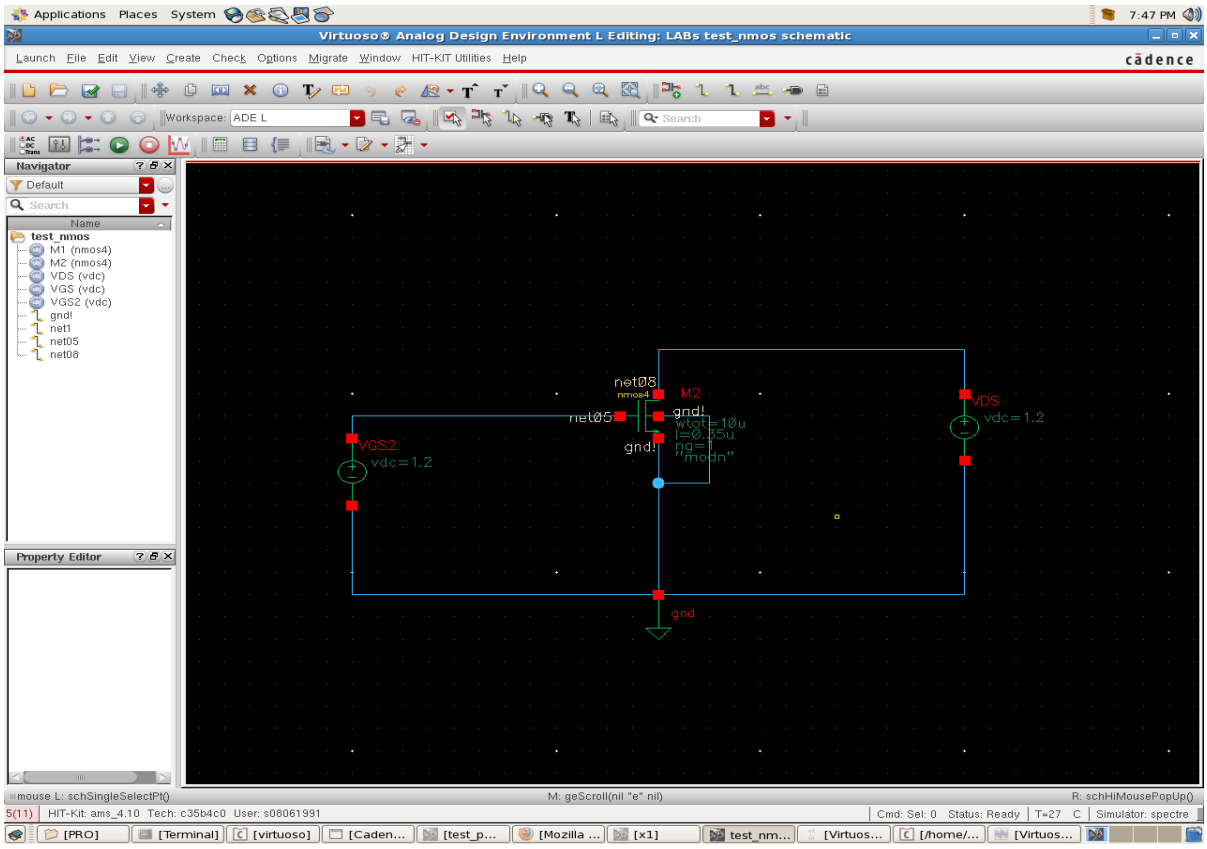

Figure-20 : Schematic of the NMOS design

The above Figure shows the schematic of our NMOS design in cadence. As said earlier, the source and body terminal are connected to the ground. A supply voltage of 1.2 V is provided to the gate terminal in order to make the transistor work. Like the PMOS that was discussed previously, we need to simulate this NMOS design to measure the threshold value like we did for the PMOS. The simulation result is shown in Figure-21

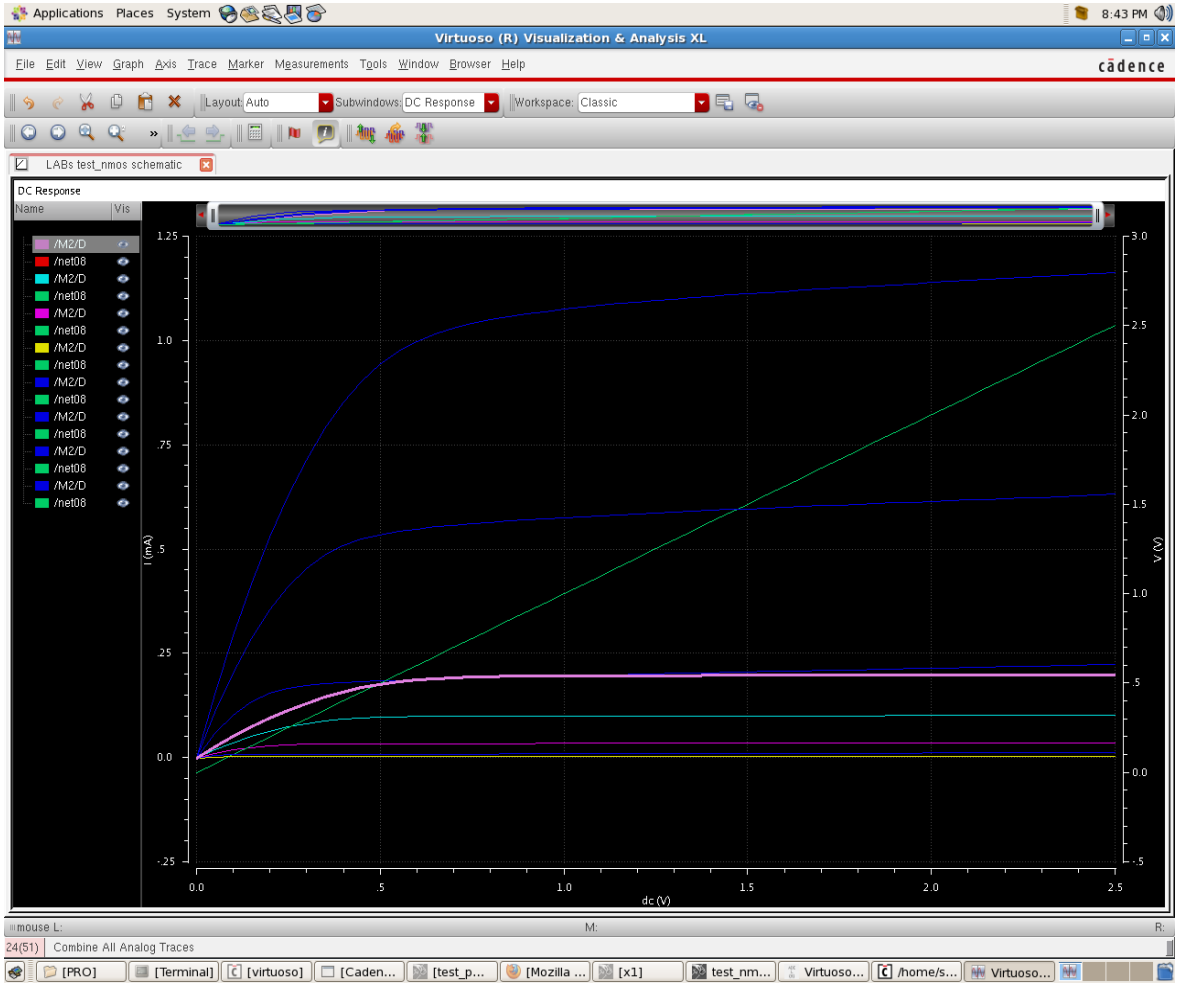

Figure-21 : Simulation result of the NMOS

The above Figure-21 shows the simulation result of the NMOS design in our schematic. The simulation result shows the graph between the Vgs (gate source voltage) and Id (drain current). The NMOS is simulated with varying Vgs. The result shows the drain current Id produced by the varying gate voltages. Thus the particular voltage at which the transistor enters saturation is said to be the threshold voltage. The common voltage at which the transistor with varying gate source voltage enters saturation is found to be 0.5V. Thus our simulation result provides us the characteristics of the MOS devices in this technology. For PMOS device, the threshold voltage is found to be 0.7V and for the NMOS device, the threshold voltage is found to be 0.5 V. Thus having studied about the requirements to design an amplifier and the characteristics of PMOS and NMOS in this chapter, we can move on to the next chapter which deals about the design of our amplifier.

CHAPTER-4

AMPLIFIER DESIGN

The chapters we discussed so far gave us an idea on the challenges for designing the amplifier, the possible types of amplifier design and the requirements for our amplifier design. This chapter will provide details of the design of our amplifier. As we go along this chapter, we can study about the design of our amplifier. There are three main stages in an amplifier. The first stage is called the bias stage. The next one is the first stage and the last one is the second stage. Figure-22 shows the structure of an amplifier design

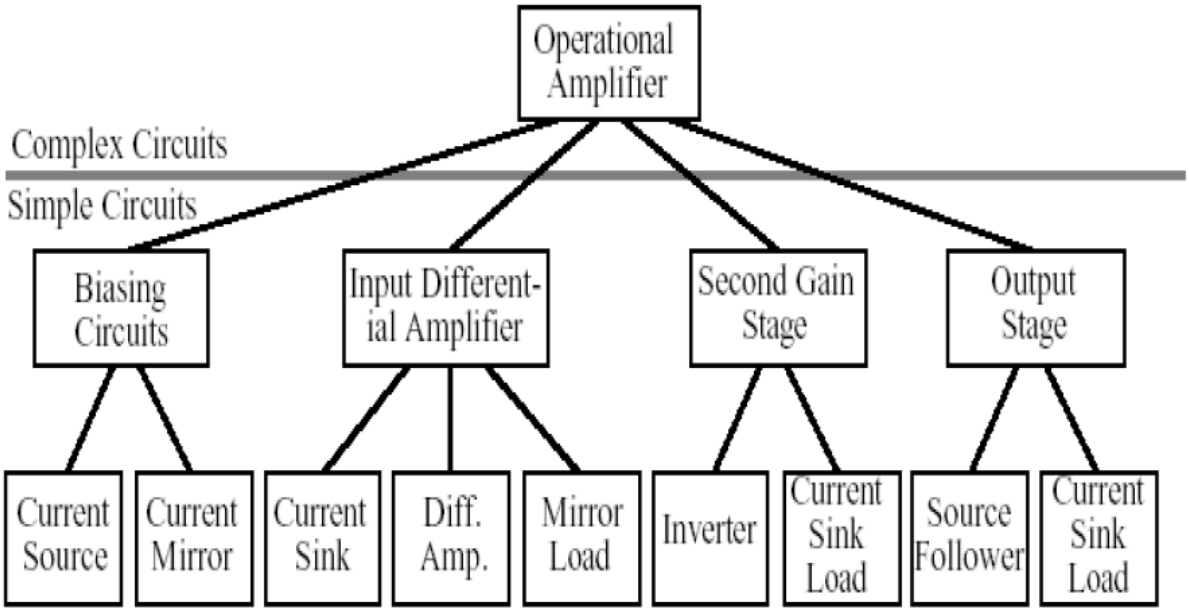

Figure-22: Structure of amplifier design[23]

4.1 BIAS STAGE:

The bias stage is the first part of an amplifier design. The main aim of the bias stage is to produce a constant voltage supply to the other two stages of an amplifier. Normally, the first stage and second stage of an amplifier needs a constant voltage that doesn't depend on the power supply. Moreover we need to provide appropriate voltages so that the transistors can be driven to the saturation region. This requirement is fulfilled by this bias stage design.

4.2 CURRENT MIRROR CIRCUIT:

The circuit shown in Figure-23 is called as the current mirror circuit. The transistors Q1 and Q2 are the two PMOS circuits. The sources of the PMOS are connected to the power supply of 3.3V. The drain of the transistor Q1 is connected to its gate terminal. Therefore, the drain voltage controls the gate voltage of the transistor Q1. This same gate voltage of transistor Q1 is provided to the transistor Q2. Hence the current produced in the drain terminal of transistor Q1 is mirrored to the drain terminal of transistor Q2. Thus this kind of circuit is called as the Current Mirror circuit. The current mirror circuit can be made with both the PMOS and the NMOS transistors. Figure-23 and Figure-24 will give us a picture on this current mirror circuit and its operation.

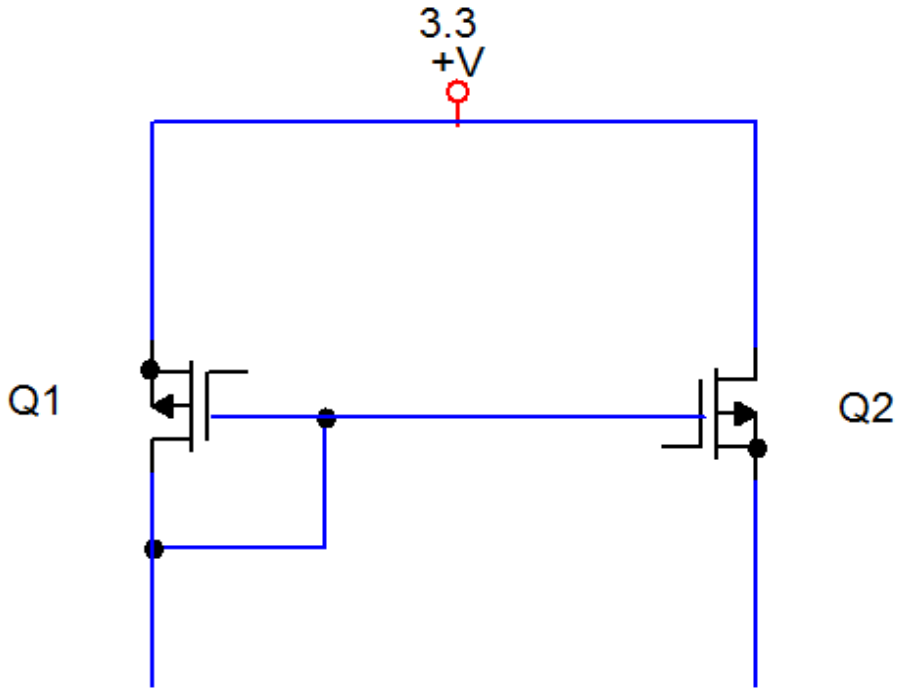

Figure--23: PMOS current mirror

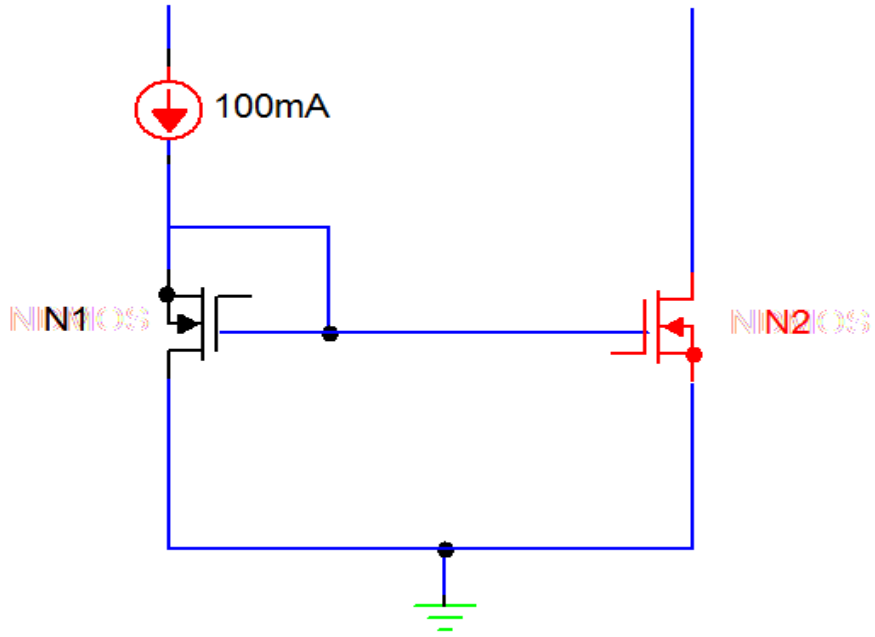

Figure-24: NMOS current mirror

Similar to the current mirror circuit shown in Figure-23 by the PMOS, we use a current mirror using the NMOS circuit. The NMOS current mirror circuit shown here has two transistors N1 and N2. The source is connected to the ground. The drain of the transistor N1 is connected to the gate of the transistor N1 and this gate voltage controls the gate of the transistor N2 and hence the current in transistor N1 is mirrored to that of transistor N2.

The PMOS is generally called as the 'current source' and the NMOS is generally termed as the 'current sink'. Hence the PMOS transistor, is used to produce the current. So if we need a device to produce a current we can use a PMOS and the produced current from the PMOS can be controlled by its W/L ratio. Similarly, as the name suggests, NMOS transistor is used to sink the produced current. Hence normally a circuit is composed of both the PMOS, which produces the current and acts as the current source and a NMOS to sink the produced current of PMOS. Thereby this combination provides us a constant current from the drain terminal of both PMOS and NMOS. Hence we need to use both the PMOS and NMOS in our circuit.

4.3 CASCODE CURRENT MIRROR:

The current mirror circuit introduced in section 4.2 provides the current that is not constant. Hence we need an approach to maintain this current steady. One such approach is the cascade method. In this cascade approach, the NMOS is cascaded with the PMOS. The remaining operation of the circuit is same as discussed earlier in this section. By this cascading method, the output current is steady.

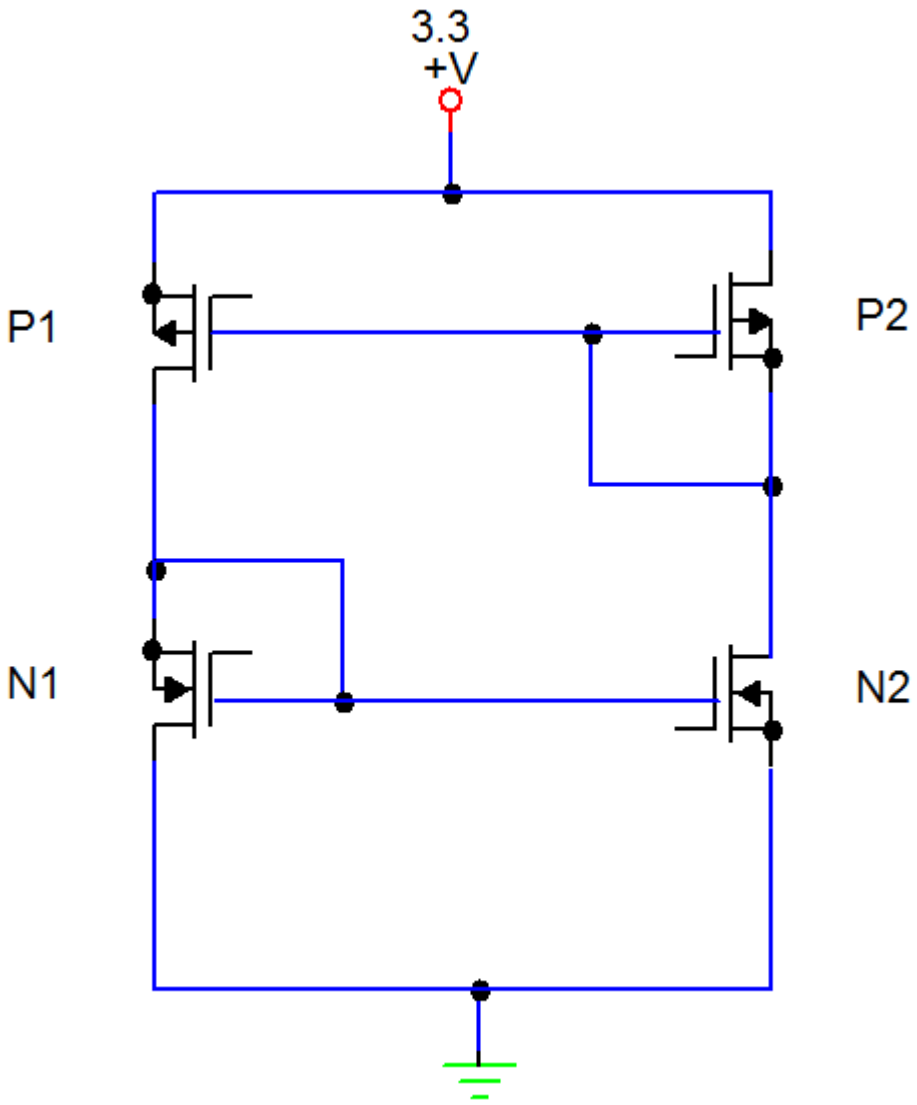

Figure-25 : Cascode current mirror

4.4: THE BIAS STAGE OF OUR AMPLIFIER DESIGN:

With this basic ideas of the bias methods, we are about to design the bias circuit for our amplifier design. The bias circuitry for our amplifier design is shown in cadence virtuoso schematic of Figure-26.

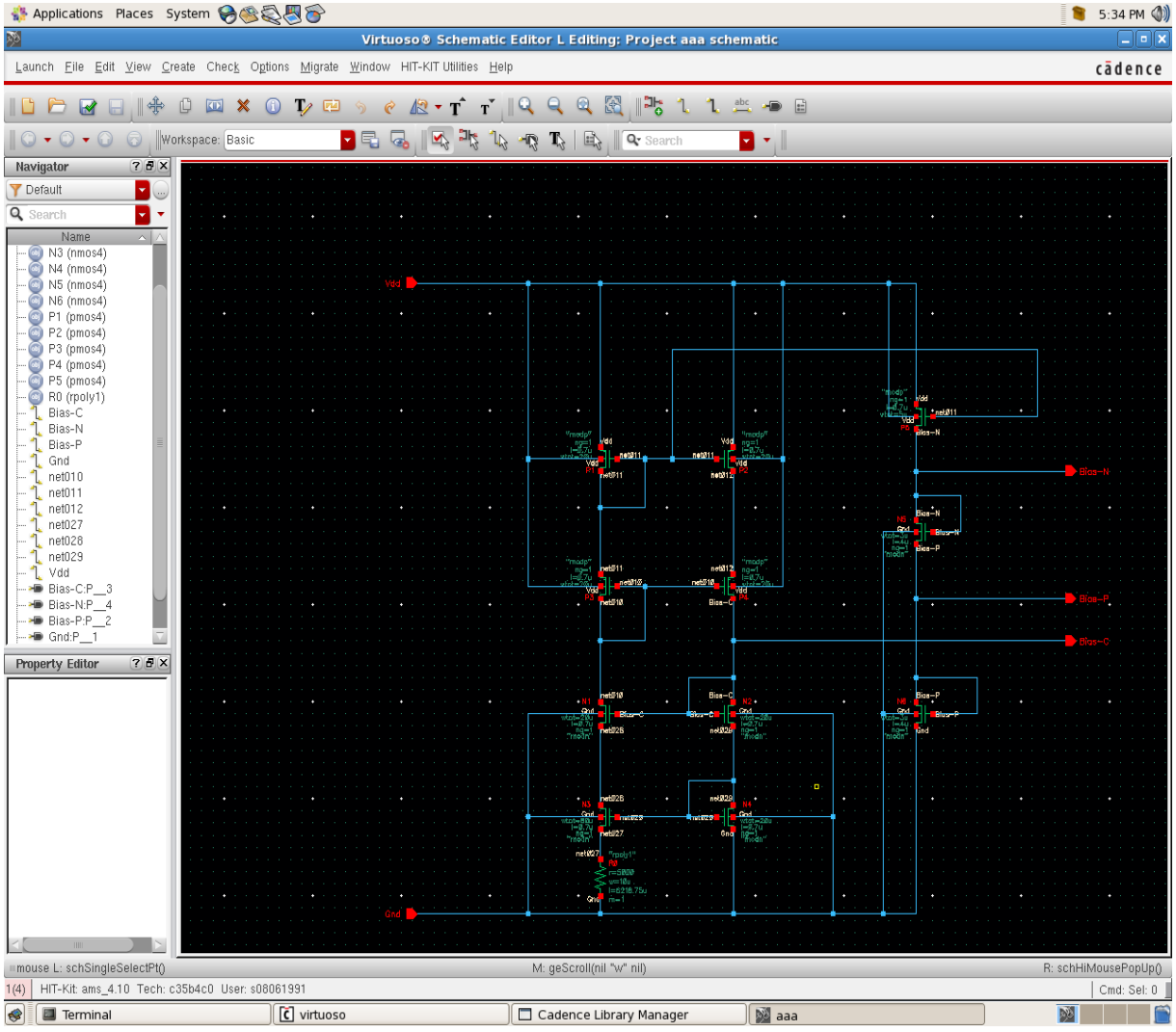

Figure-26: Bias stage design

The above Figure shows the design of our bias circuit for the amplifier design to produce a constant voltage supply.

TRANSISTOR	W/L RATIO (µ)
P1	20/0.7
P2	20/0.7
P3	20/0.7
P4	20/0.7
P5	5/0.7
N1	20/0.7
N2	20/0.7
N3	20/0.7
N4	20/0.7
N5	¾
N6	¾

Table 2 Aspect ratios of the transistor in bias stage

The above table shows the W/L ratios of the transistors that are used in our bias circuit design. The transistors P1,P2,P3,P4,N1,N2,N3,N4 acts as the main source of the bias circuitry. All these transistors are of equal width and length. Since we use a cascade of two NMOS and two PMOS transistors, the output current is steady. Also we are using a resistor of 5 KΩ to the transistor N3. The reason for adding the resistor of 5 KΩ is to increase the output resistance. In order to compensate this, the width and length of the transistor N3 is made four times higher than the transistor N4. The other transistors are of same W/L ratios. The length of the transistors is chose to be 0.7µ. This is because, in order to avoid the channel length modulation, the length of the channel is chosen as twice the minimum length of the technology. Since the technology we use is 0.35µ, twice the length is 0.7µ.

After designing the amplifier with the required W/L ratios our next step is to create appropriate input and output pins. The input pins must be created to the transistors, to which we need to apply input. One such input in is the power supply pin and also the ground connection pin. Our aim of this bias stage is to produce three constant supply voltages. Hence we need to create an output pins to the transistors from where we need to get the required output.

Now after completing the design phase in our schematic, we need to create test bench to measure the output. Creating the test bench in cadence requires a symbol view of our schematic cell view. We need to provide the required power supply voltage to find the output. The power supply and the inputs can be provided through the input pins that are created in the schematic. Similarly, the output can be measured from the output pin. Figure-27 shows the test bench of the bias circuitry.

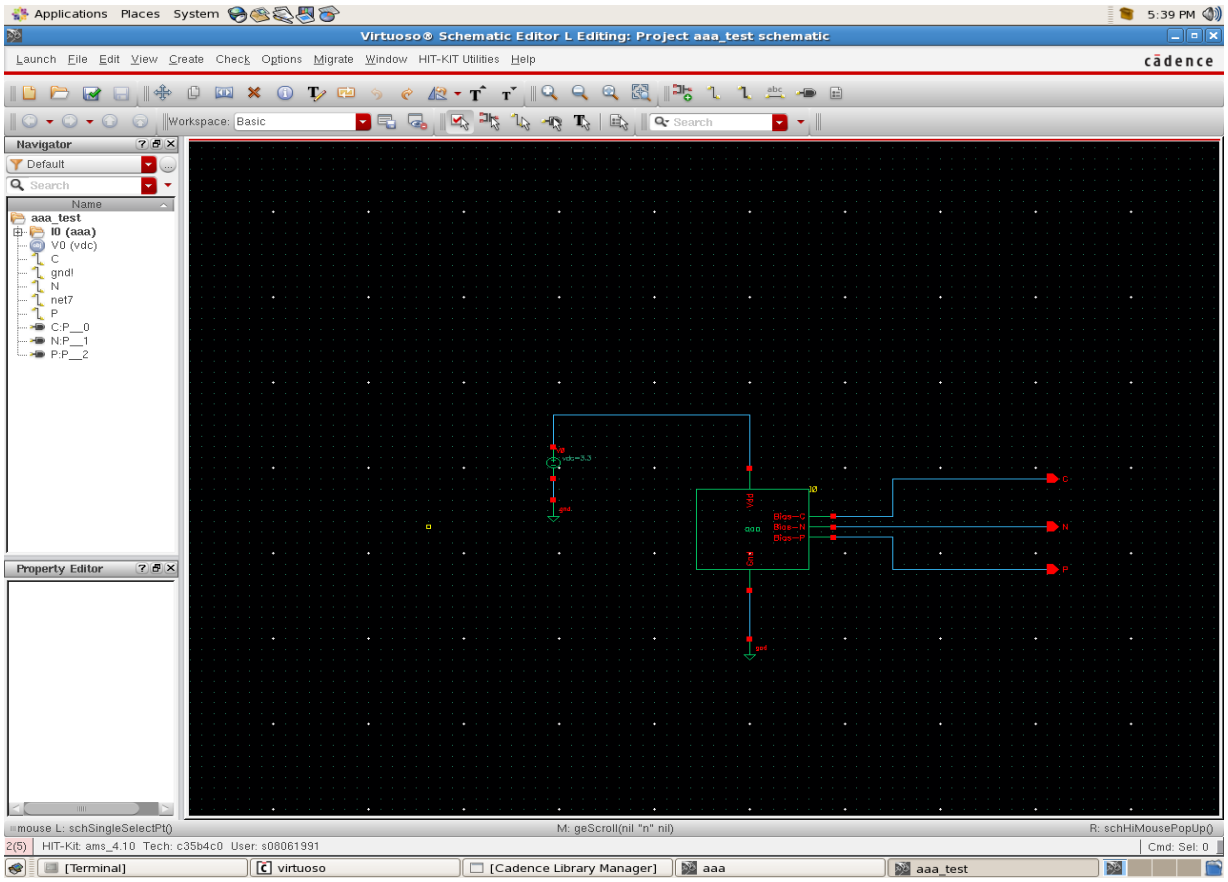

Figure- 27: Symbol view of the bias circuitry

The test bench must be simulated to measure the output. The simulation is done using the ADE-L environment in cadence. The results must be obtained from this simulation. If we have any error or if we are not satisfied with our result, then we must do some changes to our schematic design in order to get the appropriate output. Figure-28 shows the output current measured from each transistors of the current mirror circuit in the bias schematic.

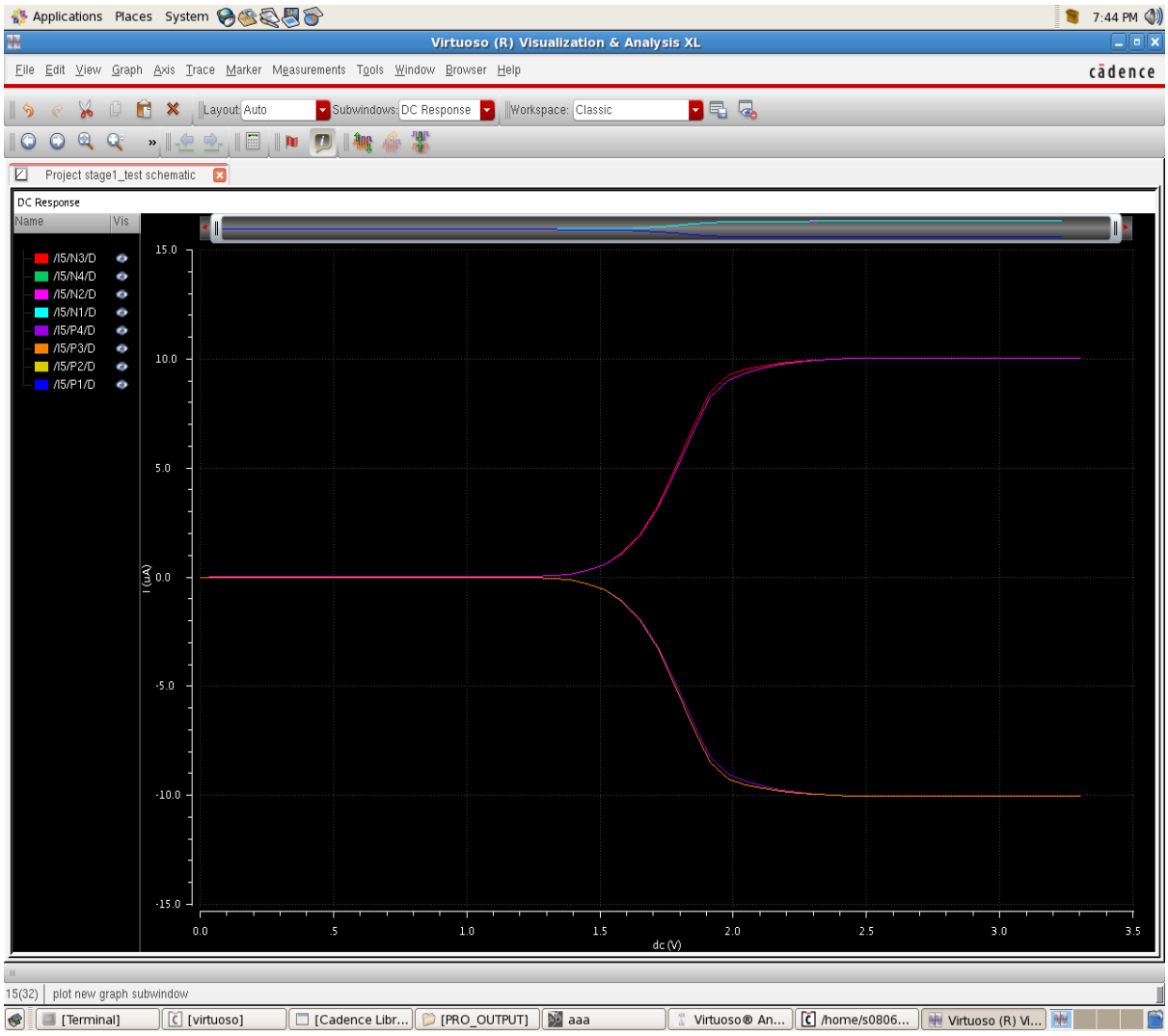

Figure-28: Output current of the current mirror circuit in the bias design.

The above Figure-28 shows the output current of the current mirror circuit from our bias design. We observe from the Figure that the current produced by all the transistors in the design is same. Hence as discussed earlier in this chapter, those circuits are called current mirror circuits as the current is mirrored. Now we need to measure the output voltages

produced from our bias circuitry. The output voltages measured from the bias circuitry is shown in Figure -29

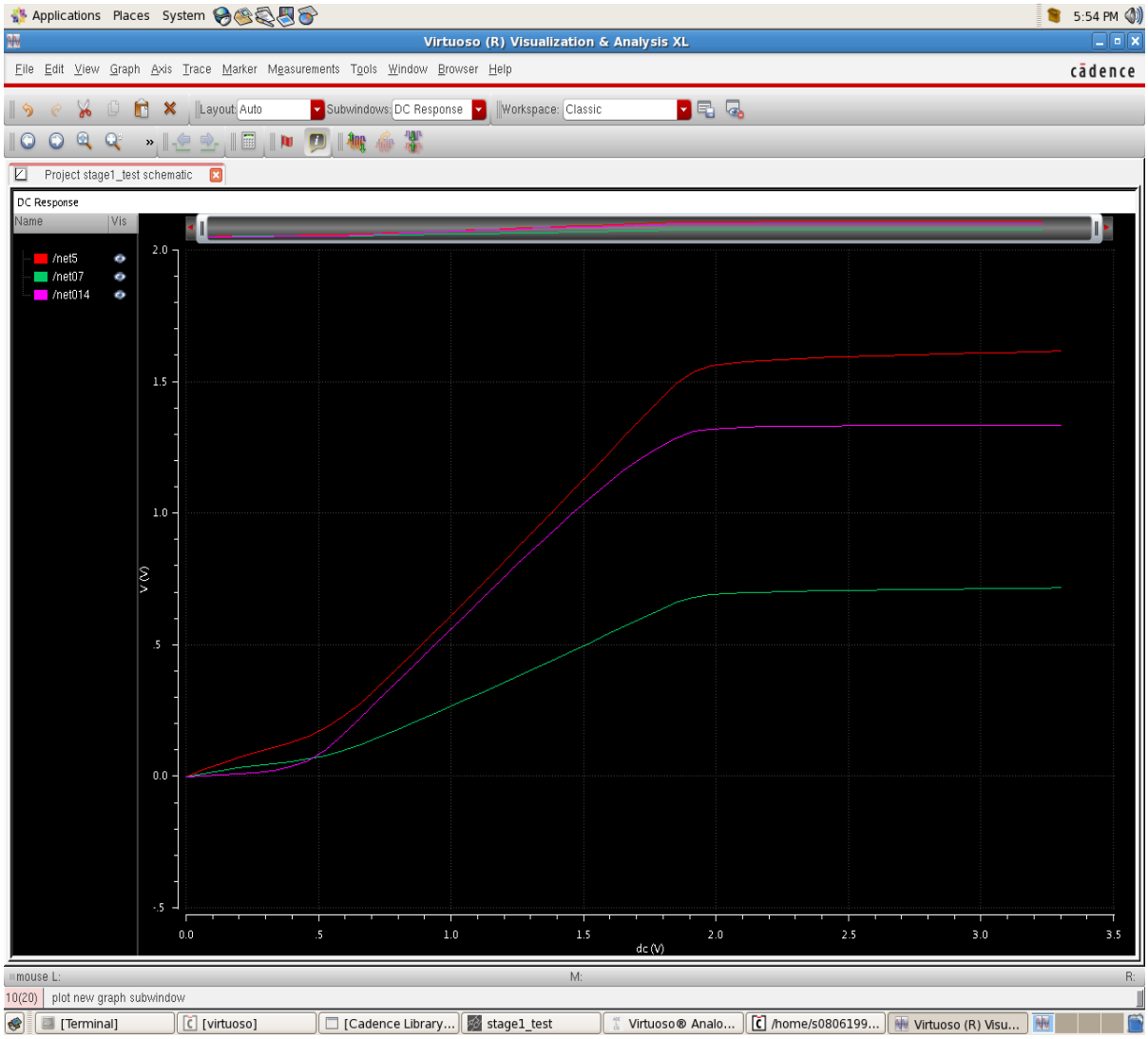

Figure-29: Output voltages of the bias circuit

The above Figure shows the output voltages measured from our bias circuitry. As expected, we could see three constant voltage supplies that are produced as the output of our bias design. The voltages that are produced from the bias circuit are 1.6V, 1.3 V and 0.7V. Figure-30 gives a better picture of this constant bias voltages.

From the cascode stage of the PMOS and NMOS circuit we get a constant voltage of 1.3V. We use a cascode of two NMOS and two PMOS because we need a good stable output

voltage. The greater the number of cascode stages, the better the chance for stability. Moreover the power supply voltage we use is 3.3V. Hence we use a 2 stage cascode for our bias voltage generation. Since all the transistors in this region are having the same W/L ratio, they all produce the same current at their drain terminal.

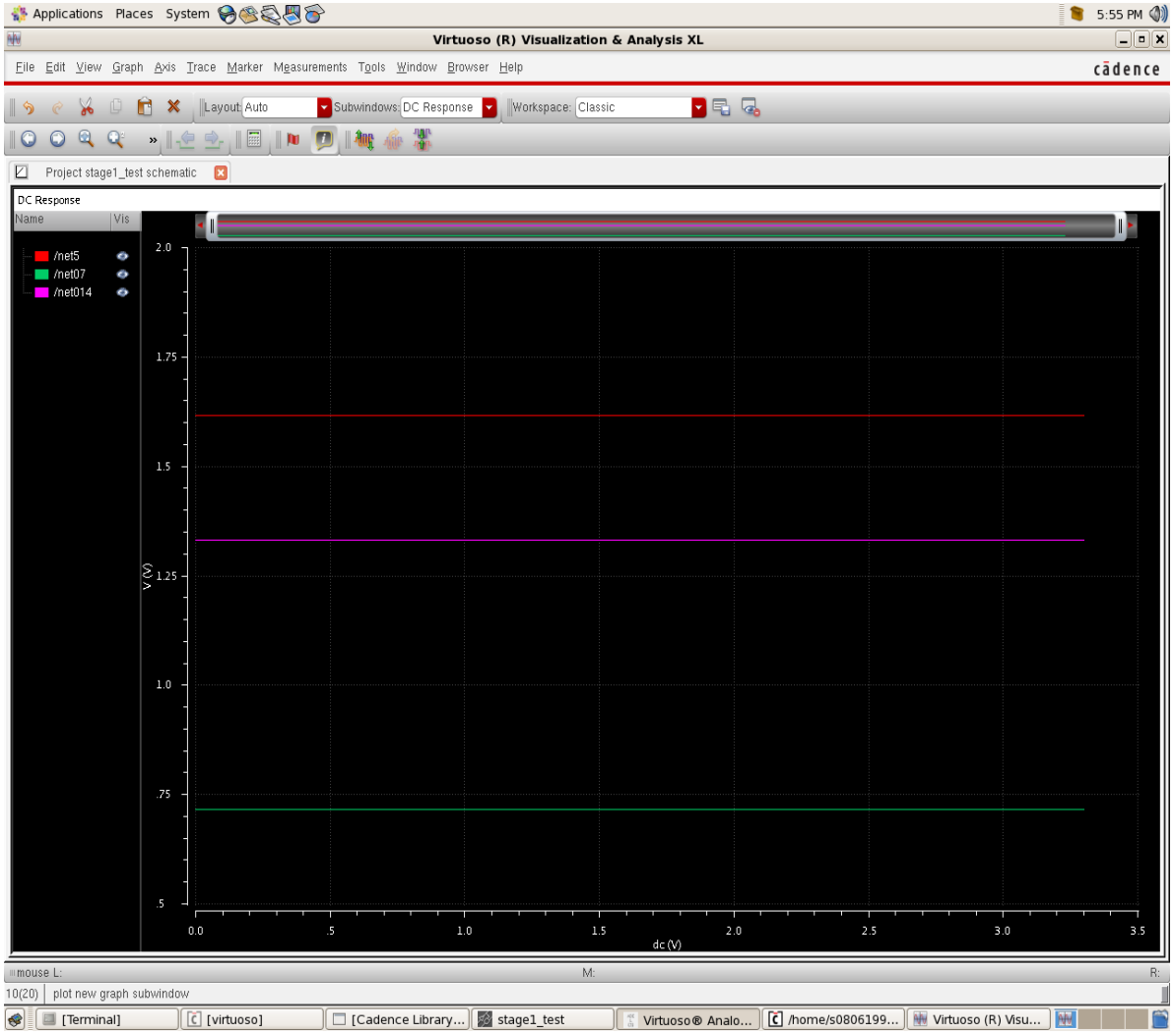

Figure-30: Constant bias voltages

The bias voltage of 1.6V produced from this cascade stage is not enough. We still need two more constant supply voltages for our amplifier design. In order to fulfill this requirement we extend this bias circuit design with one more circuit where a PMOS and two NMOS are connected. The difference between this circuit and the cascade circuit is that, for this circuit, the PMOS needs a gate voltage to be triggered ON. But in the cascode structure, we

do not need any gate voltage supply. This is because, the circuit is entirely enclosed with the PMOS and NMOS. Hence there will be some abundant voltage in the drain voltage of each transistor. This voltage is given to the gate which makes the circuit turns ON and produces the stable voltage. But in our next stage of designing the bias circuit in order to produce two more voltage supply, we don't follow the same principles of the cascade amplifier. This is because if we follow the same cascade method, we will get once again the same constant voltage. Hence there needs to be some change in the circuit design.

Hence, we design a second stage for the bias circuit so as to require two more constant supply voltage. Care must also be taken so as to not increasing the size of the circuit. Thus the second stage in our bias circuitry includes a PMOS and two NMOS. The PMOS is cascaded to the series connection of two NMOS devices. To turn on the PMOS, we provide the gate voltage from the transistors P1 and P2. This gate voltage drives the transistor P5 ON. But having P5 alone cannot produce a constant voltage. So we add a cascade of two NMOS devices to that PMOS device. Let's understand this better - If we need a constant voltage then we must increase the load resistance. Here from the design, we are about to get an output voltage from the drain of the PMOS. Hence the NMOS acts as the load to this PMOS. So we need to increase the resistance of the NMOS device. The resistance of the NMOS devie can be increased by lowering the drain current this is because from the ohm's law, current and resistance are inversely proportional. Hence we need to decrease the current to increase the resistance.

The current can be decreased by increasing the length and decreasing the width since the drain current is directly proportional to the width of the transistor and inversely proportional to the length of the transistor. Hence, we have to increase the length of the transistor and reduce the width of the transistor. It should be noted that both the NMOS must be of same W/L ratio and hence they can produce a constant current. So keeping this in mind we provide a very low W/L ratio of ¾ to the NMOS N5 and N6. Moreover it should be noted that, since we use the gate voltage of P1 and P2 to the gate voltage of P5, care must be taken in choosing the aspect ratio of the transistors. This is because change in the P5 can harm the transitors P1 and P2. Thus we have three constant supply voltages of 1.3 V, 0.7V and 1.6V andour bias stage for the amplifier is designed. The next section will discuss the first stage and second stage of our amplifier design.

4.5 FIRST STAGE OF AN AMPLIFIER:

After the design of bias stage that produces a constant bias voltage required for our amplifier design, we now concentrate on the design topology for our amplifier first stage. The aim of this first stage of amplifier is to produce a higher gain. Keeping that in mind, we can design the first stage of amplifier by choosing any one of the four available design topologies that are available. The four different kind of amplifier design topology are listed and discussed below one by one.

4.6 TWO STAGE AMPLIFIER DESIGN:

The two stage amplifier design is one of the most popular CMOS architecture. The term two stages refer to the gain of two stages. The structure of this two stage amplifier is shown in Figure-31 [23].

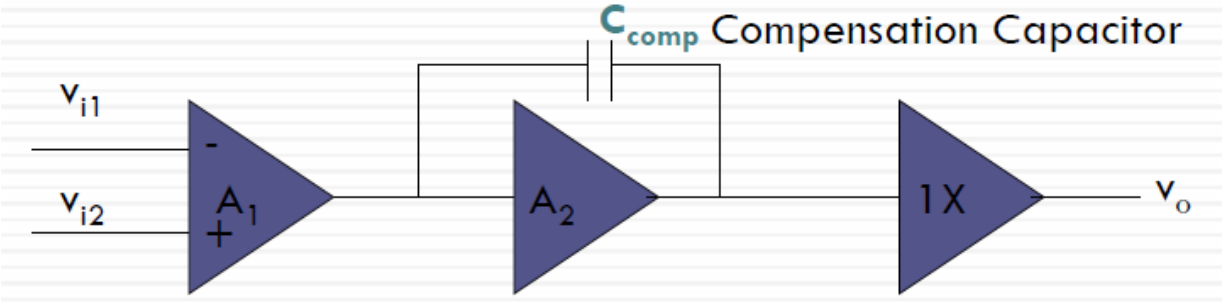

Figure-31: Two stage amplifier design[23]

The above diagram shows the architecture of the two stage amplifier. Here the first amplifier A1 is called as the first stage. The second A2 is called as the second stage amplifier and the last one is the unity buffer. The capacitor C_{comp} is called as the compensation capacitor. The output buffer stage is usually used for the resistive load at the output. The first gain stage is normally a differential amplifier with single ended or double ended. The second gain stage is the common source amplifier with an active load. The compensation capacitor is used for pole placement and so as to confirm that the op amp is stable. The first stage of the amplifier is normally designed to produce the higher gain. The second stage is added to improve the gain performance of the amplifier. The output buffer is a common source buffer stage.

4.7 FOLDED CASCODE AMPLIFIER:

The folded cascode amplifier is a type of amplifier design with a common source amplifier and a common gate amplifier connected with an opposite polarity. The folded cascode amplifier, is always considered to be a single stage amplifier. The folded cascode amplifier is also known as the operational transconductance amplifiers (OTAs). They are generally amplifiers without the output buffer. They drive only capacitive loads. The folded cascode amplifier is used to produce better gain than the two stage amplifier. But the folded cascode amplifier can consume large power consumption. The folded cascode amplifier can also be single ended or differential ended.

The folded cascode amplifier produces a high output resistance and also high common mode range. Hence they are better than the two stage amplifier in terms of gain and CMRR. The other advantage of this folded cascode amplifier is that, sometimes the load capacitance itself acts as the compensation capacitor and hence they assure the stability of the amplifier. Thus we may not need any compensation capacitor. Also, since the folded cascode stage produces high gain, we may not need a second gain stage if we are satisfied with the gain produced from this folded cascode stage.

4.8 OPERATIONAL TELESCOPIC AMPLIFIER:

The next topology of our amplifier design is the operational telescopic amplifier. Here in this design topology, the cascode structures are connected between the power supply in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along a straight line like a refracting telescope [21]. The gain of this operational telescopic amplifier is more or less same as that of the two stage amplifier. The limitation of this structure is poor output swing and poor common mode range. The main advantage of this structure is that this design topology can handle even a small signal variation faster. This topology is of only differential ended.

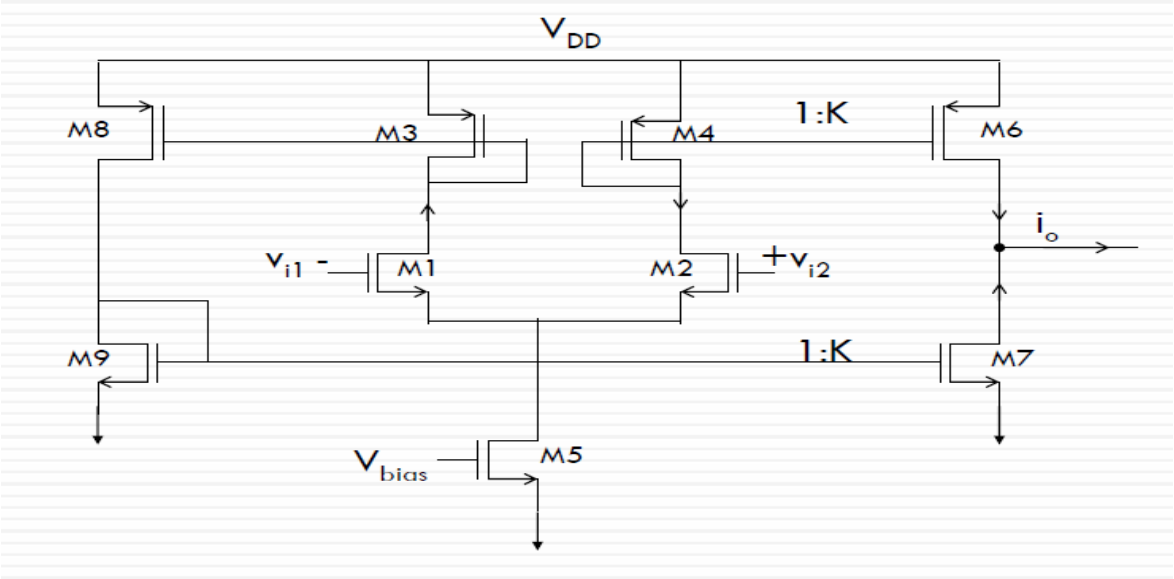

Figure- 32: Operational Telescopic Amplifier[23]

4.9 FIRST STAGE OF AMPLIFIER DESIGN:

By learning about the all the available design topologies, we now design our first stage of the amplifier from one of these topologies as base. From the above analysis, we choose the folded cascade topology for our amplifier design as it can produce the higher gain and higher common mode range than the other topologies. The schematic diagram of our first stage of amplifier is shown in Figure-33.

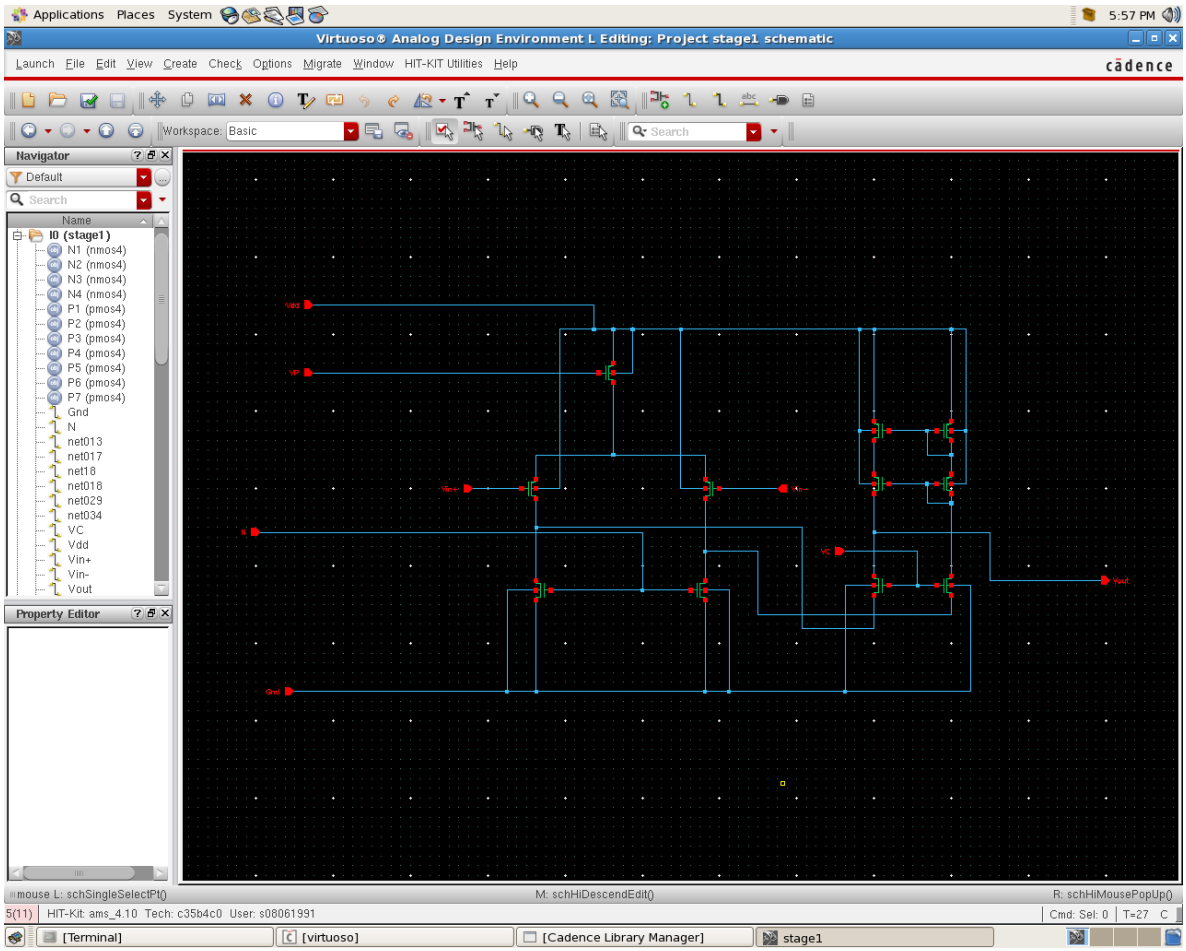

Figure-33: First stage amplifier design

The above Figure shows the schematic representation of our first stage amplifier design. Similar to the bias circuit design, we must specify the transistors width and length for its operation. The width and length of the transistor devices is provided in the Table[3]

TRANSISTOR	W/L RATIO
P1	1/0.7
P2	15/0.7
P3	15/0.7
N1	25/10
N2	25/10
P4	15/5
P5	15/5
P6	15/5
P7	15/5
N3	5/1.4
N4	5/1.4

Table 3: Aspect ratios of the transistors in the first stage design

From Figure-33, we could find that the transistors P2 and P3 are the input transistors. The input is provided to the gate terminal of these transistors. The transistor P2 and P3 sources are connected together. The sources of the differential input transistors must be connected to a current source. As said earlier, a PMOS acts as the current source. Hence we connect a PMOS transistor P1 to the sources of the differential input transistors P2 and P3. In order to make the transistor P1 ON, a bias voltage must be produced to the gate terminal, so that it turns ON. This is done by creating a pin to the gate terminal of this transistor. The bias voltage can then be provided in the test bench. The source of this transistor is connected to the power supply of 3.3V. Now by adjusting the W/L ratio of this transistor, the required current is produced through the drain terminal. It is to be noted that the length of the transistor is chosen to be 0.7 µ. This is because the transistor P5 in the bias circuitry also has the same length. Hence the transistor P1 in the first stage is also chosen with the same length so as to avoid the problems during the layout of this amplifier design.

As said earlier, the transistors P2 and P3 acts as the input of the amplifier design. This is chosen because, PMOS transistors acts better to flicker noise than the NMOS transistor. Hence the input is given to the gate terminal of these transistors. The drain terminal of the PMOS transistors cannot be connected to the ground directly. Hence we connect two NMOS transistors N1 and N2 to the drain terminal of this input transistors. This is because as discussed earlier, NMOS acts as the current sink. The sources of the transistors N1 and N2 is connected to the ground. A bias voltage must be given to the gate terminal of the transistors N1 and N2 to make the transistors ON. Thus a pin is created to this gate terminal.

Our topology of amplifier design is the folded cascade design topology. Hence to fulfill this design topology, we need to make a folded cascade structure of this amplifier design. In order to accomplish this, the drain terminal of the transistor pairs P2 N1 and P3 N2 is connected to the source of the transistors N3 and N4. Thus a folded cascade structure of our amplifier design is made. Because, the input transistors are PMOS whereas the transistors to which the output of this connected is a NMOS transistors. Thus a folded cascade structure of our amplifier design is made.

To turn on this folded cascade pair of transistors N3 and N4 we need a voltage to the gate terminal of this folded cascode transistor pair. Thus another voltage pin is created to this gate terminal. The PMOS current mirror pairs of transistors P6 P7 and P4 P5 is added as a cascode structure to this folded cascode transistor so that it acts as a load to this transistors. The W/L ratios of the current mirror pair is chosen so as to produce better result at the putout. As discussed earlier, we choose higher length for this current mirror pair.

Thus the schematic design of our first stage of the amplifier design is over. Now we need to design a test bench for this amplifier design and test the circuit. The test bench of this schematic design can be made by creating a symbol design. The test bench design of our first stage amplifier is shown in Figure-34. From this test bench design, we can measure the outputs.

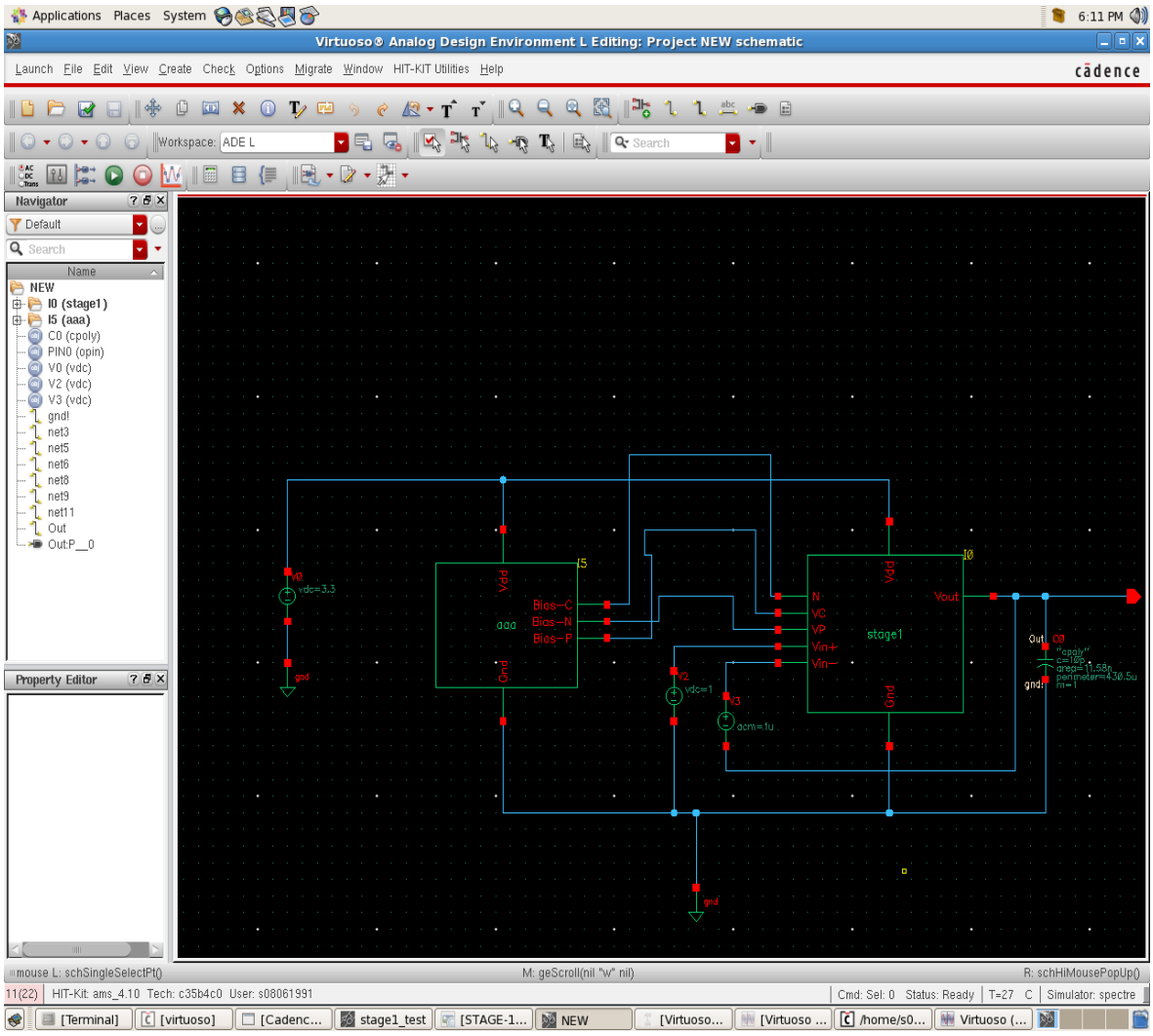

Figure-34: Test bench of amplifier first stage

The above Figure-34 shows the test bench for the amplifier first stage design. The bias stage and the first stage design are connected together. The constant bias voltages from the bias circuitry are given to the voltage pins that are created in our schematic design. The positive and negative input terminal of the transistor in first stage is connected to the inputs as shown. The positive terminal of the first stage amplifier is connected to a dc voltage supply of 1V. To the negative supply voltage an AC signal of very low voltage of 1µV is used. The AC signal is provided to the negative terminal as the feedBack. The output of the first stage amplifier can be found by using the capacitor load. A capacitor load of 10pF is used in the output terminal to measure the output gain of the first stage amplifier.

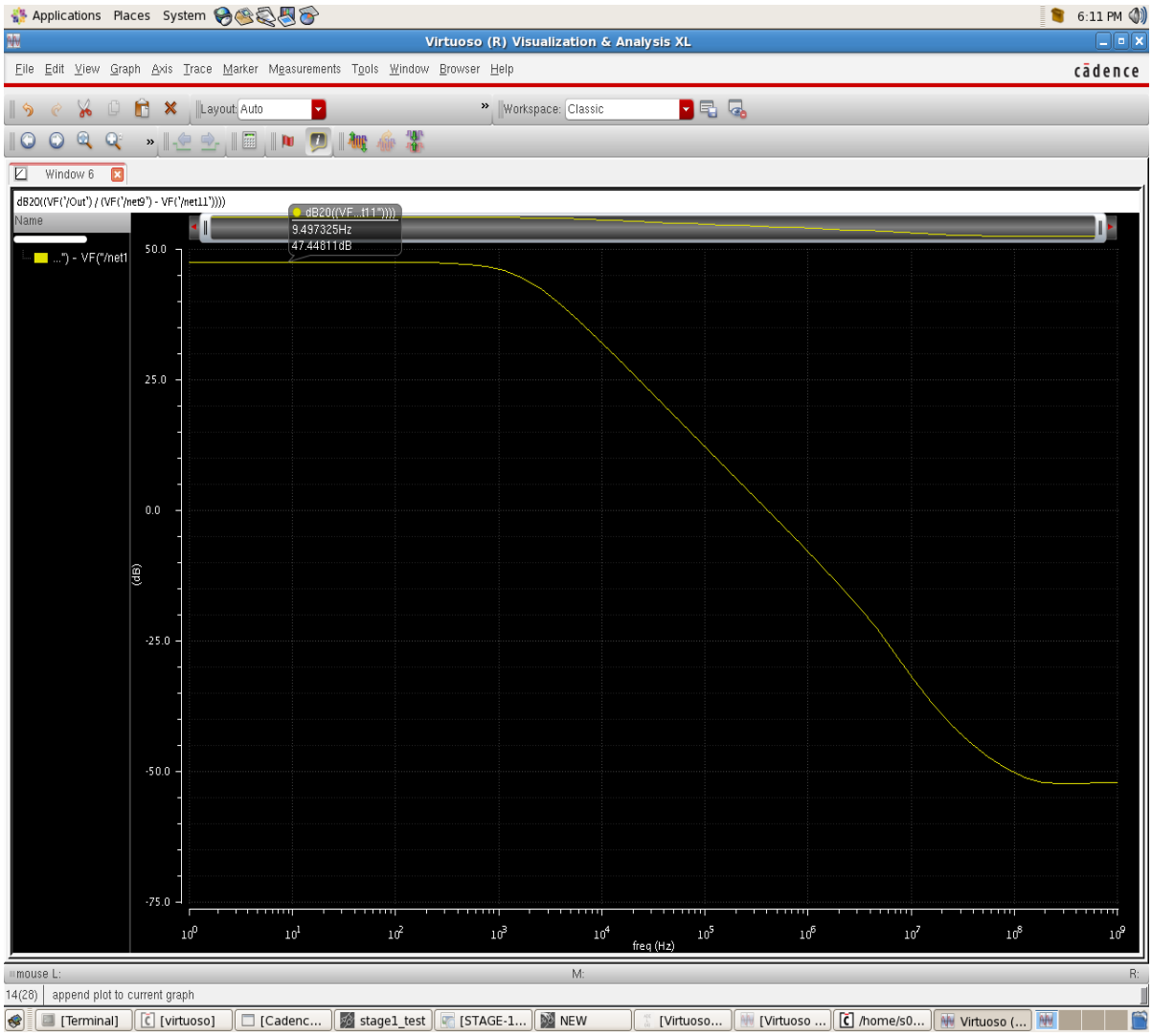

Figure-35: Gain of the first stage amplifier

The above Figure-35 shows the measured output gain of the first stage amplifier. It is measured from the graph that the output gain of the first stage amplifier is around 48 dB. But this measured gain is not enough for our amplifier design so we need to improve the gain of this first stage amplifier. To increase the output gain we can either increase the gain of the folded cascode stage by adding one more PMOS current mirror pair. But by adding this extra circuit, the NMOS transistor pairs N3 and N4 are driven to the triode stage. So an alternative approach must be needed to solve this issue. Hence we go for another stage of amplifier design, the second stage.

4.10 SECOND STAGE OF AMPLIFIER:

Following the first stage of the amplifier, we go for the second stage which is to be designed to increase the gain of our amplifier design. As discussed earlier, a second stage of the amplifier means a second gain stage and it is designed to improve the gain. The second gain stage is of common source amplifier. Figure-36 shows the design of the second gain of the amplifier.

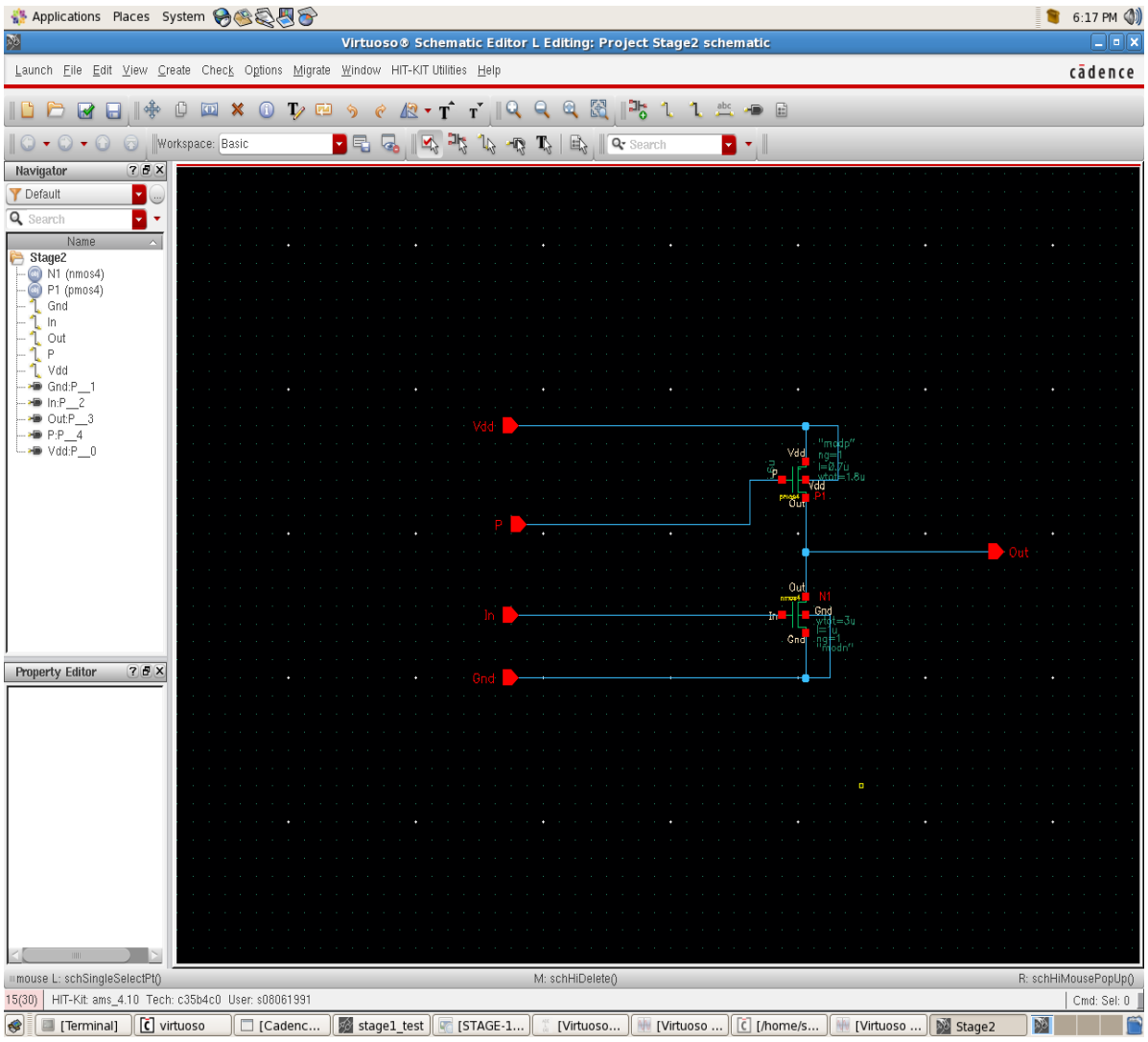

Figure-36: Schematic design of second stage

TRANSISTOR	W/L
P1	1.8/0.7
N1	3/1

Table 4 Aspect ratios of transistor in second stage

The second stage of the amplifier consists of a PMOS and an NMOS. The gate voltage of the PMOS P1 is the same bias voltage that is used to drive the drain terminal of the transistor P1 in the first stage of the amplifier. The output of the first stage amplifier acts as the gate voltage and input to the NMOS N1 in the second stage. The length of the transistor P1 is made same as that of the transistor P1 in the first stage of the amplifier in order to avoid the problems in the layout. Now the test bench for the entire amplifier is to be designed in order to measure the output results. The test bench of the amplifier design with the bias circuitry, first stage of the amplifier and the second stage of the amplifier is shown in Figure-37. The output measured with the capacitive load of 10pF. The measured output results are produced.

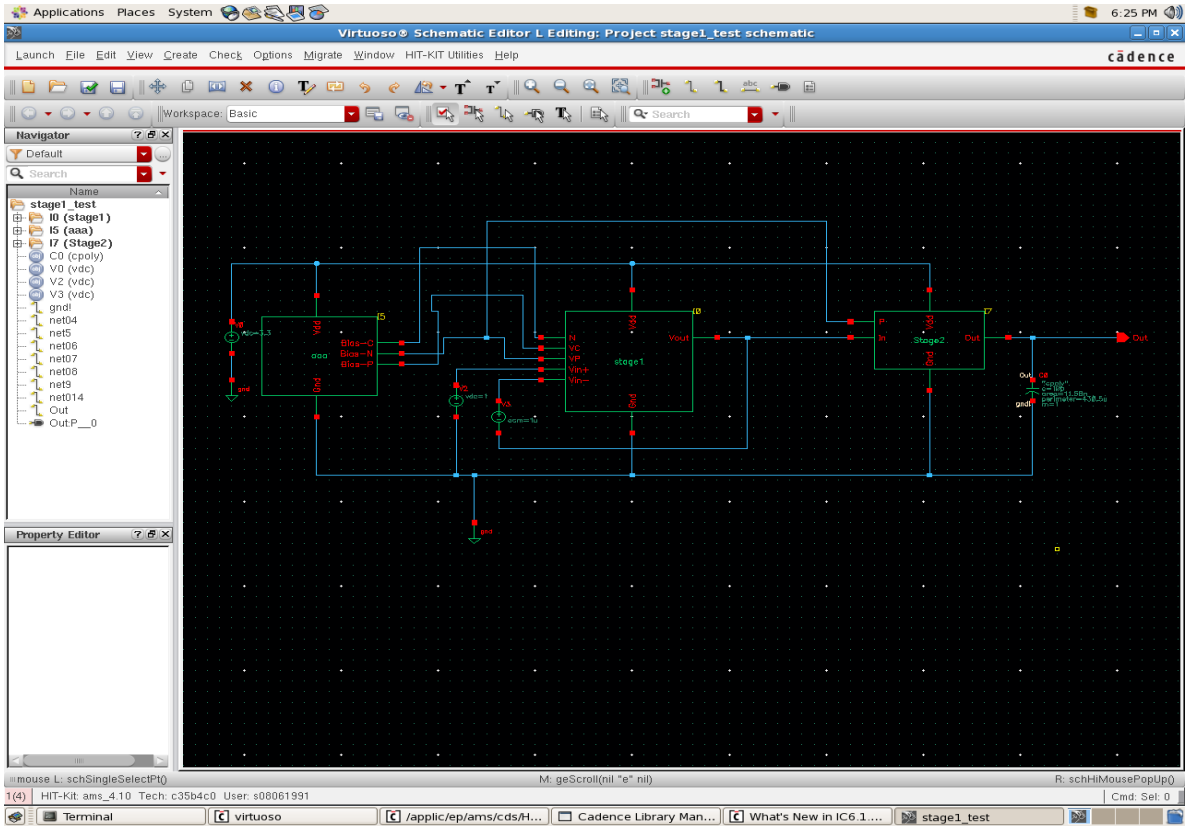

Figure-37 test bench of the complete amplifier design

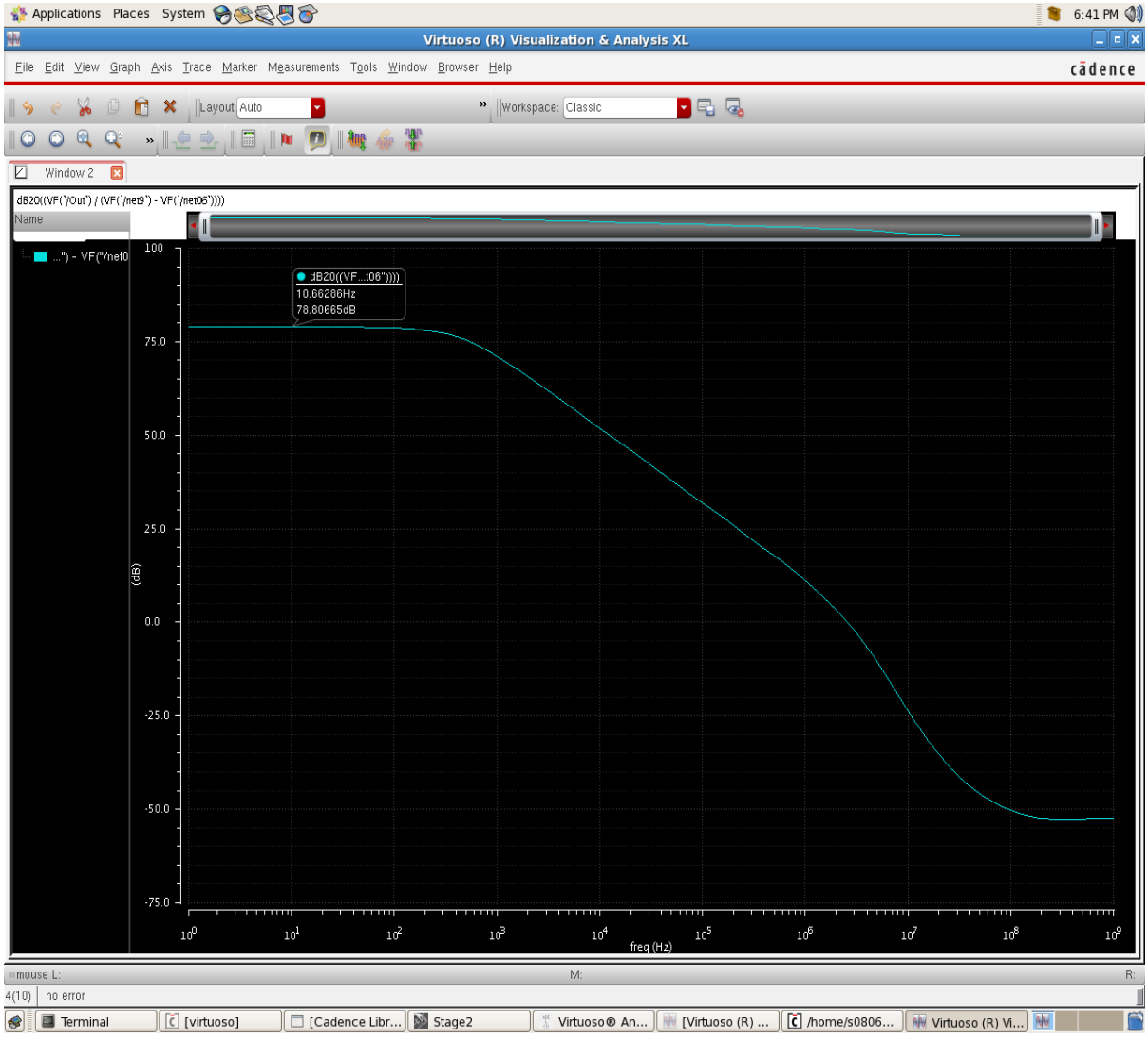

Figure-38: Gain of the amplifier

The above Figure-38 shows the output gain measured from the test bench that was shown in the previous Figure. The measured gain of the amplifier is around 78 dB and this gain is a good measure. Now the stability of the amplifier must be taken into consideration. Hence to find the stability of the amplifier, we must measure the phase margin of our amplifier design. Figure-39 shows the measured phase margin of our amplifier design.

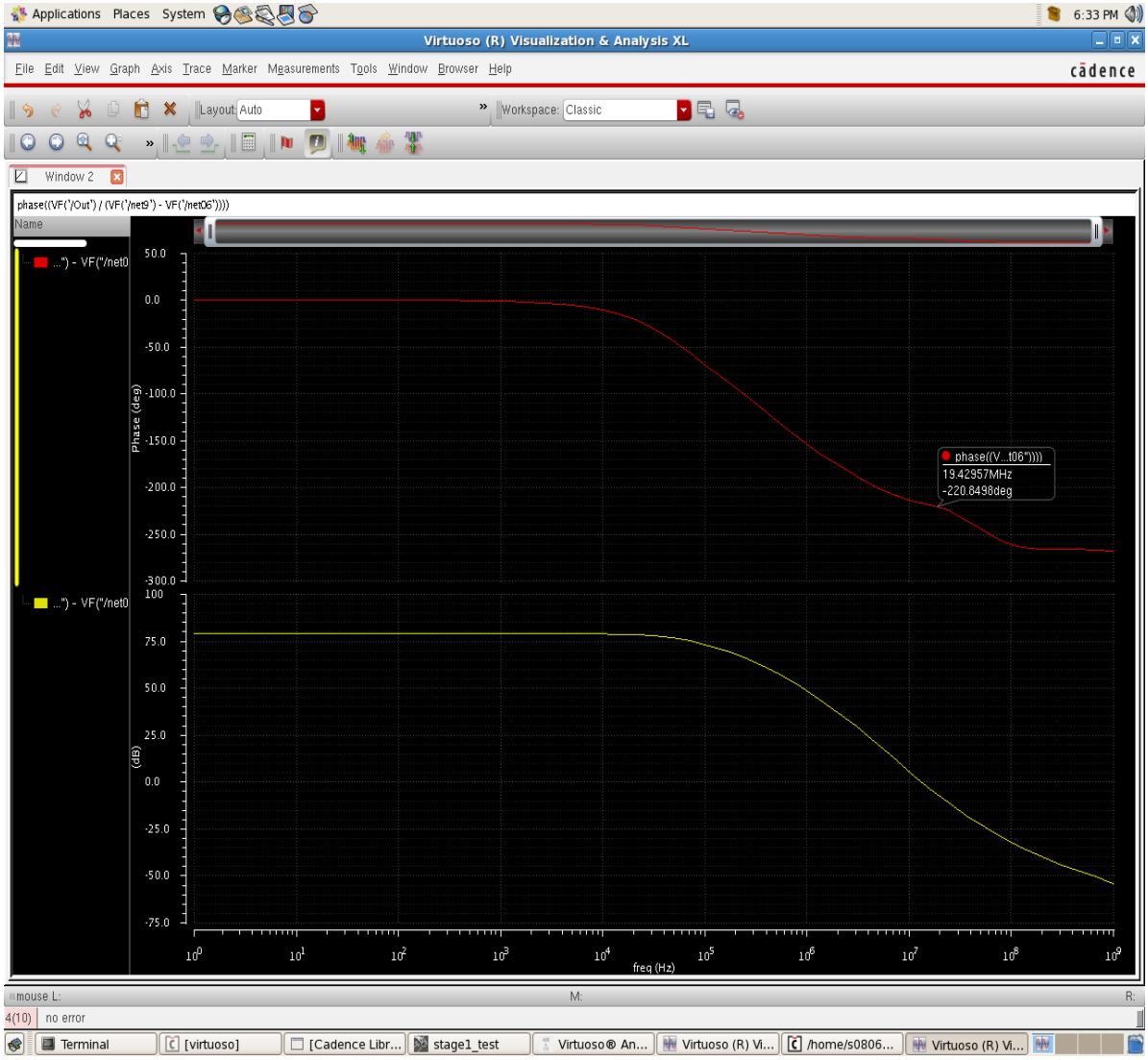

Figure-39: Measured phase of the amplifier design

The above Figure shows the measured phase margin. To have an easy understanding, we split the gain and the phase margin. The Figure above with red output is the phase margin and the Figure below in yellow is the gain of the amplifier.

The stability of the amplifier must be measured by the pole placement. The pole must be measured as follows. The 0 dB of the gain must be measured. A straight line must be drawn from the 0 dB of the gain and the intercept of this 0 dB line with the phase margin must be measured. This measured value is the pole of the amplifier. This pole must be residing less than 180^{o}. So, if the measured pole is less than 180^{o} then the amplifier is said to be stable.

If the pole is not below the 180^{o} then it means the amplifier is not stable and hence we need some changes in the design.

From Figure-39 we measure that the pole is placed at 220^{o}. Hence the amplifier we designed is unstable and hence we need to make the amplifier to be stable. In order to make the amplifier stable, we need a compensation capacitor. The use of this compensation capacitor is for the pole placement. Hence a compensation capacitor must be added to the second gain stage of the amplifier. Figure-40 shows the improved second gain stage.

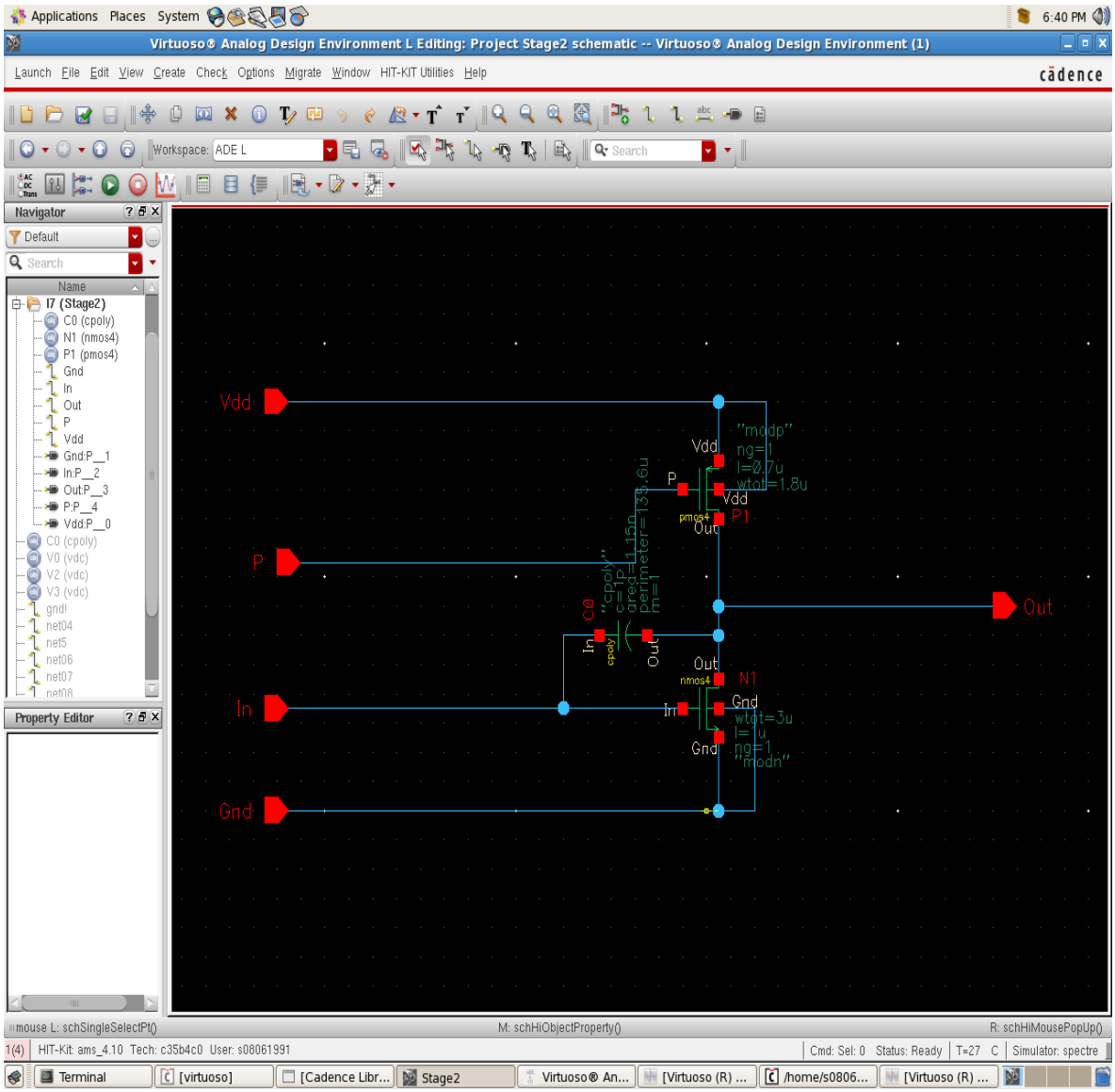

Figure-40: Compensation capacitor

The above Figure-40 shows the improved second gain stage with a compensation capacitor. A compensation capacitor of 1pF is added to the NMOS transistor. Now, the gain and the phase margin of the improved amplifier design is measured. The result is shown in Figure-41

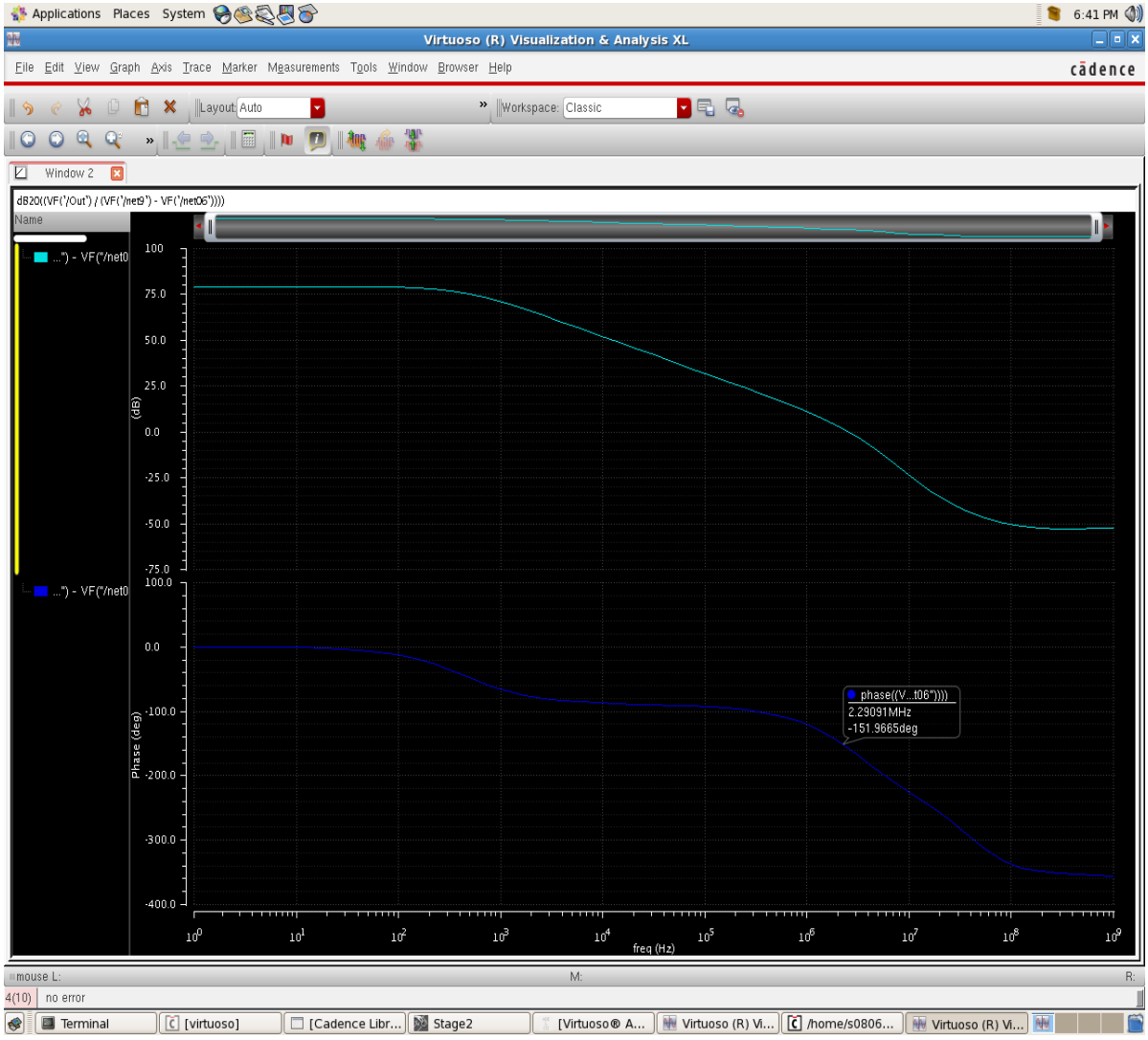

Figure-41: Improved phase of the amplifier

The above Figure-41 shows the output of the improved amplifier design. The gain of the amplifier is still measured to be 78 dB. The pole placement is now measured to be 150^{o}. Now the measured pole is less than 180^{o}. Thus the amplifier is now in a stable situation.

Thus the amplifier we designed has the gain we required and the amplifier is also stable. Now we have to perform other tests to our amplifier design.

4.11 OFFSET VOLATGE MEASUREMENT:

After ensuring the required gain and the stability of the amplifier, we now focus on the offset voltage measurement. Figure-42 shows the method of offset voltage measurement.

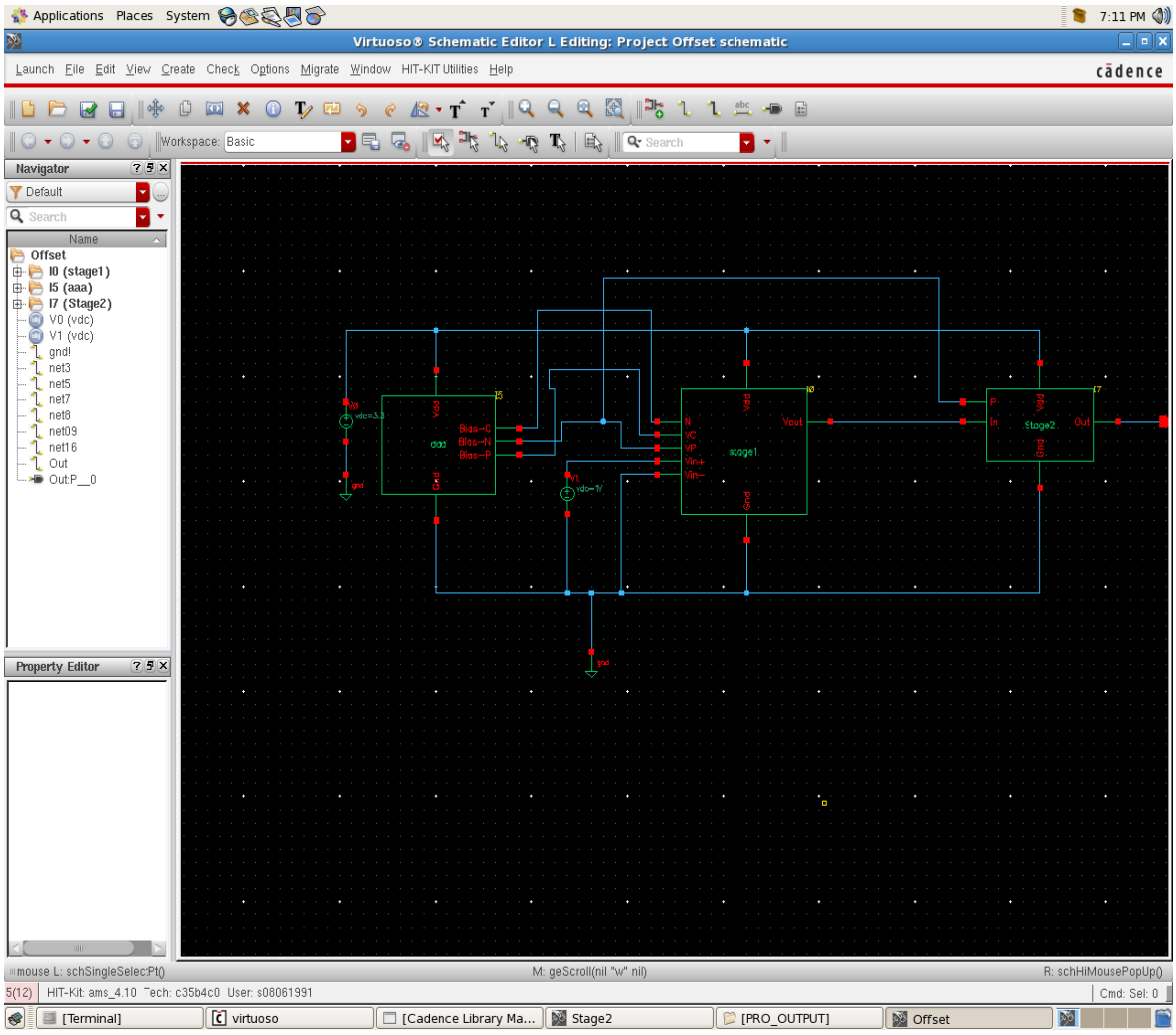

Figure-42: Setup to measure offset voltage

Figure-42 shows the amplifier setup for the offset voltage measurement. A DC voltage source is provided to the positive input of the amplifier and the negative input is grounded. Now the output of the amplifier is measured and this gives us the measured offset of our amplifier design.

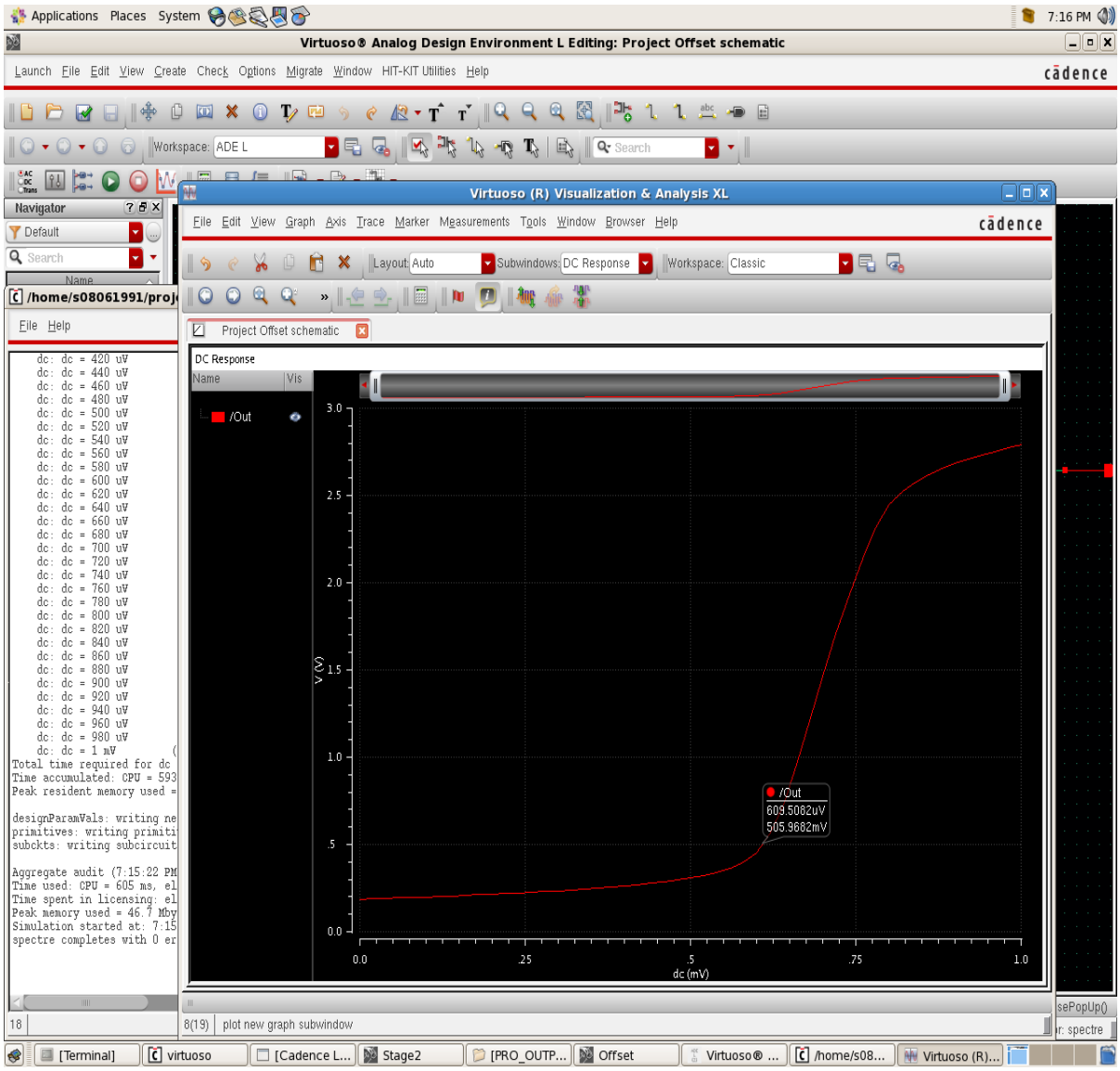

Figure-43: Measured offset

Figure-43 shows the measured offset voltage of our amplifier design. The offset voltage is measured with the voltage sweep of 1mv. The measured offset is found to be around 0.5mV..

4.12 CMRR CALCULATION:

Now we can calculate the common mode rejection ratio (CMRR) measured by our amplifier. From Equation [23], we can write the equation of CMRR as below

$$\text{CMRR} = 2(gm1(ro2\ parallel\ ro4)Rss) \qquad \text{Equation (23)}$$

From our design of the amplifier, we can find the required parameters for our amplifier design. By using the dc annotate option in cadence, the parameters of the transistor like the transconductance (gm), drain current (Id), drain source voltage(Vds), overdrive voltage(Vds) and threshold voltage (Vt) is displayed. The below gives an example of how this appears.

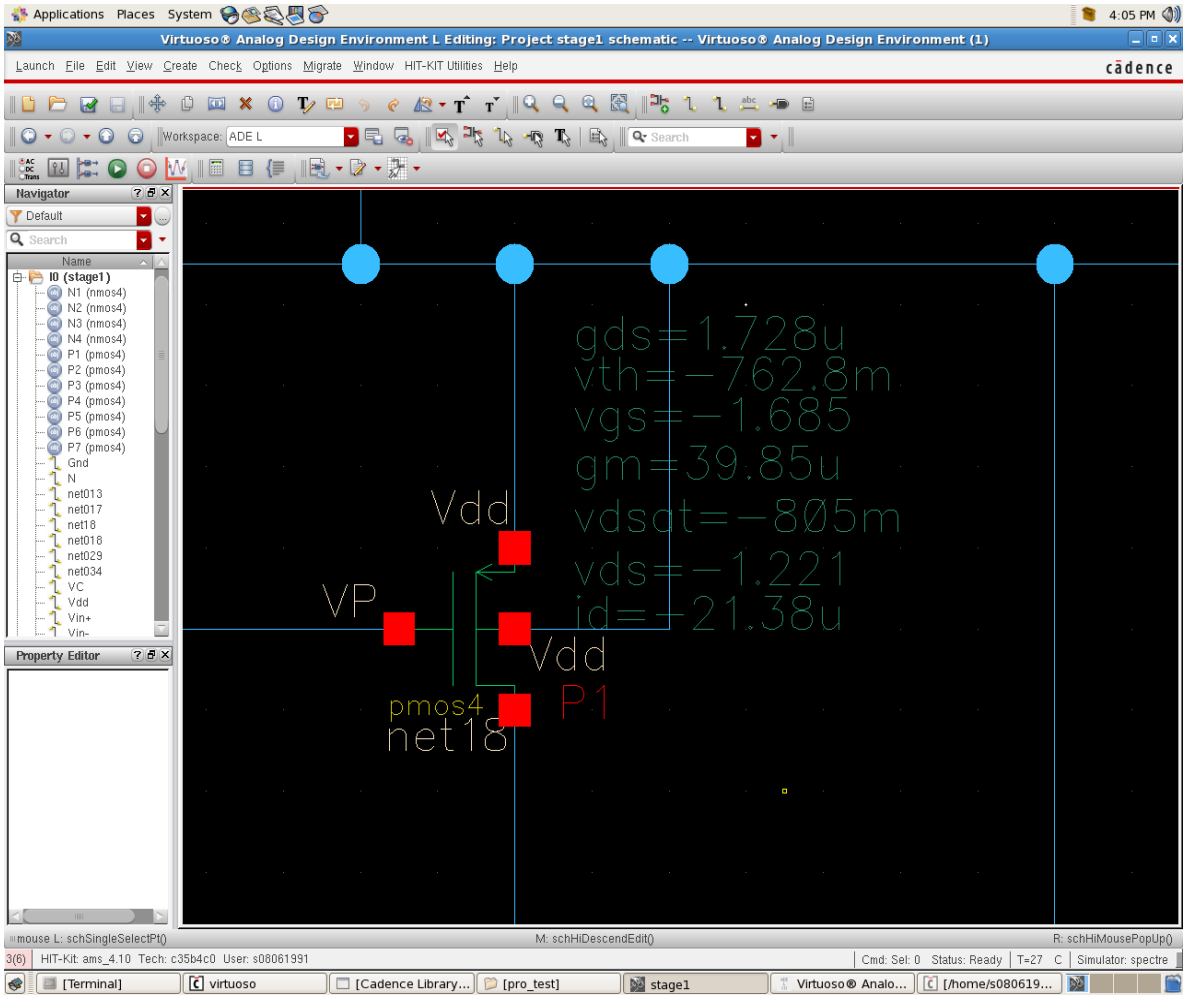

Figure-44: Amplifier displaying the values

Since the transistors are in saturation, we need to find the output resistance for each transistor. The output resistance can be found as below in equation (24)

$$ro = \left(\frac{1}{gds}\right) \qquad \text{Equation (24)}$$

From our amplifier design, the following transistors are considered to find the CMRR. The value of gm1 is found from the input transistor P2. Similarly, the ro2 and ro4 are found from the transistors P3 and N2 respectively. The Rss is the resistance of the tail current source P1.

gm1 = 132.3µ

ro2 = 1/gds = 1/(877.7n) = 1.14MΩ

ro4 = 1/gds = 1/(350.1µ) = 2.85KΩ

Rss = 1/gds = 1/(1.72 µ) = 578.703KΩ

On substituting these into the equations, we get

CMRR = 216.847K

Or when expressed in decibels, we can write it as

CMRR = 20 log(216.847K)

CMRR = 106.72 dB

Thus the amplifier we designed has produced the required CMRR that is necessary for our amplifier design. Hence our amplifier has produced the required gain and CMRR.

4.13 POWER CONSUMPTION:

The power consumption in an amplifier can be measured by the product of the current consumption at all branches of the amplifier and the supply voltage. The supply voltage is 3.3 V. The sum of the current produced at all branches is found to be 40.9µA.

Power = V*I

Power=40.9µ * 3.3

Power = 135µW. A detailed explanation on this power dissipation is studied in the next chapter.

CHAPTER 5

CONCLUSION

This thesis provides detailed information of the amplifier design. The thesis started with the introduction of the concept of bio potential signals. Chapter 2 provided a picture of the challenges that concern the design of our amplifier especially about the flicker noise. The chapter also provided us the different techniques that are available to overcome this flicker noise. The next chapter provided us the list of requirements that is needed for the amplifier design. The chapter also provided us the target values that are required for our amplifier design. Chapter 4 provided us the various design topologies that is available and the design of our amplifier. The result and their analysis were also provided in that chapter. Thus the amplifier we designed produced the following results shown in table [5].

PARAMETER	VALUE
TECHNOLOGY	AMS 0.35µ
POWER SUPPLY	3.3 V
GAIN	78 dB
CMRR	106 dB
POWER CONSUMPTION	135µW

Table 5: Result produced from our amplifier design

From the above table we could view the final results produced by our amplifier design. The amplifier we designed produced the required gain and CMRR with the power supply of 3.3 V. The only factor that concerned the design of our amplifier is the power consumption. The amplifier we designed produced a power consumption higher than we expected. This is because the topology we used to design the amplifier is the folded cascode topology. The folded cascode topology consumes more power than the other topologies that were

discussed. But still we chose the topology so that it can produce better gain and CMRR than the other topologies. As expected our amplifier produces the required gain and CMRR and lack the power consumption. Moreover the power consumption is increased when we add a second stage in order to increase the gain.

5.1 SUMMARY AND ACHIEVEMENTS:

- The whole project was implemented in Cadence, which is an analog design tool. Analog design and simulations of amplifier were made and the simulation results were produced.
- Understanding the necessary to design an amplifier for EEG signals amplification.
- Understanding the key concepts in amplifier design like how the design can be and what are the available topologies to design our amplifier.
- Understanding the trade offs in amplifier design like area, power and noise.
- Understanding the various methods how we could combat noise like using the PMOS input stage and higher aspect ratios.
- Making use of the various analog design environment simulation tools like DC, AC, noise, gain and phase to make better understand of the amplifier design.
- The lectures and labs from module EE6622 Analog ASIC design by Dr.Brendan Mullane was helpful in understanding the analog design and doing this project.
- The characteristics of PMOS and NMOS were studied to make our amplifier design easy.
- The need for bias stage and producing constant supply voltages for the amplifier design. Current mirrors were used to produce the constant supply voltage.
- The first stage of an amplifier was designed using the folded cascode topology and a significant gain was achieved.
- The need to improve the gain and thereby building the second stage of the amplifier which is a common source amplifier.
- To make the amplifier stable we use a compensation capacitor.
- Achieved a working CMOS amplifier design that can be taken further in future work in a limited time frame.

5.2 LIMITATIONS:

My original designated Thesis project area was on a totally separate topic to this work carried out, however I very much wished to perform an analog CMOS design topic instead to gain expertise in this area of VLSI. This new amplifier project started with the aim of designing the complete chopper amplifier beginning proper in the middle of February much later than expected – however it became clear that due to time constraints, the project could not proceed forward with the full implementation of the entire chopper amplifier stage. Hence the project focus was changed to design of a CMOS amplifier within the Chopper architecture and the simulations were carried to confirm the working specification. The layout of the amplifier was not drawn due to the time constraints.

5.3 FUTURE WORK:

The amplifier design can be improved by reducing the power consumption. The design can be tried with other topologies to produce the required gain and CMRR and to consume less power. Moreover efforts can also be made to construct the amplifier with the power supply voltage of 1.8V. The same design can also be constructed using the other technologies and their results can be compared. The amplifier can be further developed with the implementation of the chopper stage. The entire amplifier design can then be made to layout and fabrication. The noise simulations were also carried out using the analysis→noise option in the ADEL environment. But we couldn't get the possible result. This is because the noise model and setup in the AMS 0.35µ technology could be the reason. This can also be tried for further improvement of this amplifier. The next section will provide a basic idea of about how the chopper stage can be built and the specifications that should be considered in designing the chopper stage.

5.3.1 BUILDING CHOPPER STAGE:

We discussed about the various types of chopper stage that are available in the chapter-2. From the discussed chopper stages, we can choose the 'Closed Loop Chopper Stabilization Amplifier' for building the chopper stage as it is an advanced chopper design when compared with the other three. The table below can provide us the necessary specifications that are to be considered for building the chopper stage.

SPECIFICATION	VALUE
AMS	0.35µ
Supply Voltage	1.8 V- 3.3 V
Gain	75dB
CMRR	100dB
Power	50µW
Chopper Frequency	1-4 KHz
Low Pass Frequency	150 Hz
Input referred Noise	< 2 μV_{RMS}

Table 6: Specifications that can be made for Chopper Stage

The above table provides us a target value that can be achieved in future with the development of the chopper stage. The power supply is reduced. This is because in future, we can use a differential amplifier method rather than a single ended amplifier method. By doing so, we can reduce the power. Also, we choose higher chopper frequency. This is because choosing higher chopper frequency can help in eliminating the flicker noise. Because higher the frequency, lesser will be the flicker noise. The low pass corner frequency is chosen as 150Hz. The signals from the electrode are of frequency 100Hz. So when this signal enters into the chopper stage they should be of noise free. Hence we choose the low pass corner frequency of 150Hz, so that the signals below this frequency will be cut down and this filtered signal will then be modulated. The next section will discuss about a new parameter called NEF.

5.3.2 NEF:

NEF is an acronym of Noise Efficiency Factor. Noise efficiency factor is an important parameter in determining the noise performance of the amplifier. Due to small frequency bandwidth of the bio potential signals, it is the target noise level that defines the power

dissipation of the bio potential amplifiers[1]. The noise in the amplifier increases as the number of noise sources increases. Hence we need to achieve more power to achieve the required target level[1]. The NEF can relate the noise and power dissipation. The lesser the NEF value, lesser will be the power dissipation value. The noise efficiency factor can be given by the equation (25) and equation (26) [25].

$$NEF^2 = V_{RMS}\left(\frac{2gm}{4KT\pi BW}\right) \quad \text{Equation (25)}$$

$$NEF^2 = V_{RMS}\left(\frac{2Id}{4KTVt\pi BW}\right) \quad \text{Equation (26)}$$

Where,

V_{RMS} is the total input referred noise of the amplifier.

BW is the 3dB bandwidth of our amplifier.

Id is the drain current

Vt is the threshold voltage

Thus a basic idea for building the chopper stage was discussed. With the help of this the chopper stage can be designed along with the amplifier we designed in this project.

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